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ABSTRACT

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This report describes the purpose and function of plasma instrumentation designed and built by M. I. T. for use with Mariner A spacecraft. The equipment determines the particle-number density and energy spectra of plasma protons and electrons, and the direction of motion of the plasma. The basic sensor unit is a faraday cup which measures a current produced by the proton or electron component of the plasma. The energy of the protons or electrons which reach the collector is determined by potentials applied to the grids. The energy spectrum of the protons or electrons can be determined from the measured collector current as a function of an incremental grid potential. By using several collectors which face in different directions, it is possible to study the directional properties of the plasma flow. The instrument contains four faraday cups whose fields of view lie in a plane and are mutually perpendicular. Each faraday cup, in sequence, measures proton or electron current as a function of retarding voltage.

The electronic circuits which operate the sensors are discussed in detail. For convenience, the circuits are divided into three sections, the measurement link, the high-voltage supply, and the logic. The measurement link receives a modulated signal (10^{-12} to 10^{-7} amp at 2 kcps) from the faraday cup collector and amplifies, compresses, and demodulates it to present a DC output signal to the spacecraft Data Automation System. The high-voltage supply contains a modulator which produces a 2-kcps square wave of variable amplitude (approximately 10 to 3000 volts) which is applied to the faraday cup grids. The sequence of operations in a measurement cycle is controlled by the logic circuit which is in turn controlled by the spacecraft Data Automation System.

Author

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GLOSSARY

β	feedback term	R_{eg}	equivalent grid noise resistance
C	capacitance (farads)	R_f	feedback impedance
e_o	output signal voltage	R_g	grid impedance
E	voltage	R_l	load resistor
E_{in}	input voltage	R_s	source impedance
E_o	output voltage	T	absolute temperature
E_{max}	maximum voltage increment	V	voltage
f_o	output frequency	V_d	diode voltage
gm	transconductance	V_i	minimum voltage
H	transfer function	V_o	maximum voltage
I_b	anode current	W_r	resistor energy
I_c^2	screen current	W_o	constant
K	Boltzmann's constant	Z_{in}	input impedance
K_{gain}	gain factor	Z_{out}	output impedance
Q	transistor	Δf	small frequency change
q	electrical charge	Θ	variable phase angle
R_a	input resistance	Φ	phase

MARINER A PLASMA PROBE

I. INTRODUCTION

A. General

The study of the nature of interplanetary gas is one of the major areas that can be studied using earth satellites and deep space probes. In a qualitative sense some properties of this medium are reasonably certain. The gas is mostly hydrogen which, out to distances of several astronomical units from the sun, must be nearly completely ionized. This ionization is a consequence of the large flux of solar radiation in the short-wavelength region regardless of whether the sun itself is the main source of the gas. As a result of the high degree of ionization, the gas behaves as a plasma; furthermore, its behavior is determined entirely by collective phenomena produced by long-range electric and magnetic forces rather than by collisions between individual particles of the gas. Because of the high conductivity of the plasma, and the large distances over which physical effects take place, magnetic fields are effectively "frozen" into the medium. As a result of this coupling (providing the kinetic energy density of the bulk motion of the plasma is large compared to the magnetic energy density) the magnetic field is carried along with the plasma; if the reverse is true, the magnetic field energy density dominates, and the magnetic field controls the possible bulk motions of the material.

Experimental results from Russian space probes and Explorer X show that the first condition exists in the region near the earth, i.e., at about one astronomical unit from the sun. The measured particle fluxes were about 10^8 and 10^9 cm^{-2} sec^{-1} and the bulk velocity about 3×10^7 $cm\,sec^{-1}$ directed away from the sun.

B. Objectives of the Mariner A Plasma Experiment

At least four separate fields of research are directly related to studies of plasma properties.

Verification of Acquired Data:— The physical parameters which characterize the medium must be known in detail. Among the most important of these are the particle fluxes and their energy spectra In this connection, it should be noted that bulk velocities in the range of 10^7 to 10^8 $cm\,sec^{-1}$ correspond to proton energies of a few kev; however, the energy of the electrons which corresponds to this bulk motion is only a few ev. Assuming the temperature of the plasma to be only moderately high (say 10^4°K) the thermal kinetic energy of the electrons will exceed the energy of bulk motion. Therefore, the electrons are expected to have a roughly isotropic velocity distribution and to be carried along by the protons. Moreover, the energy spectrum of protons and electrons may not be Maxwellian and, because of the slow exchange of energy between

electrons and protons, it is very unlikely that there is equipartition of energy between these components at the position of the earth.

Solar Physics:– A more detailed knowledge of the properties of the plasma and, in particular, a knowledge of the spatial and thermal variations of these properties, should provide some clues to the origin and mode of formation of the plasma. If, as seems almost certain, the plasma has its origin in the coronal activity of the sun, these studies may provide information leading to a better understanding of the corona itself. Correlation of magnetometer and plasma measurements may determine how magnetic fields are generated by, and propagated from, the sun. All these questions are of interest not only for investigations concerning the sun but for related astrophysical problems.

Theoretical Magnetohydrodynamics:– There is at present no general agreement on a theoretical treatment of the interplanetary plasma, given even the same initial assumptions. To a great extent, this situation is a result of the inherent mathematical difficulties. Almost certainly a great deal of progress will be made when some experimental data are available. It is well to remember that one experimental difficulty in laboratory studies of magnetohydrodynamic phenomena is that of scale. A great many phenomena are masked or completely modified by "wall effects," and it is certain that some studies are easier to carry out in space than on Earth. A thorough understanding of the behavior of the plasma in space will undoubtedly have application in terrestrial laboratories.

Interaction of Plasma with the Geomagnetic Field and Associated Solar-Terrestrial Relationships:– Since the plasma cannot penetrate the geomagnetic field, except possibly in the polar regions, a boundary exists between the magnetosphere and the interplanetary region. A study of this boundary region is of great importance and is best done using satellites. Nevertheless, a knowledge of what impinges on the geomagnetic field is a necessary part of the problem and for this a space probe is the best instrument.

To summarize, the intent is to investigate the particle densities (number per cc of electrons and protons), their differential energy spectra up to 4 kev, and the spatial and thermal variations of these quantities. The information will be correlated with data concerning the associated magnetic field and applied toward the solution of the problems just outlined.

II. SYSTEM DESCRIPTION

A. Description of the Plasma Probe

The instrument, which has been developed at M.I.T., is basically a faraday cup mounted in the skin of the space probe. A measurement of the proton current could, in principle, be made simply with a grid covering a hole in the outer conducting skin, and behind it a collector plate kept sufficiently negative with respect to the grid to repel the electrons. With the cup facing toward the plasma the protons of the plasma would flow to the collector, the electrons would flow to the grid or to other parts of the vehicle body, and a net measurable positive current would be observed at the output of the collector. However, this measurement is not possible when the cup faces the sun (an interesting direction for plasma observations) because there is a photoelectric current of the order of 10^{-8} amp/cm^2 emitted from the collector (Hinteregger, 1959). The sign of this current is the same as that of the proton current.

Although this photocurrent can be suppressed easily by placing another grid in front of the collector and maintaining it a few tens of volts negative with respect to the collector, there remains a reverse photocurrent produced by light reflected from the collector onto this suppressor grid. Photoelectrons emitted from the suppressor grid and traveling to the collector produce a current which subtracts from the proton current. This reverse current can be as much as one-tenth of the maximum direct proton current expected, and would invalidate the measurement of all but the highest proton current densities. This difficulty is overcome by modulating the plasma current using an AC field, without modulating the reverse photoelectric current.

Figure 1 is a diagram of the type of probe used, showing the arrangement of grids. Grids 5 and 2 are kept at the potential of the vehicle skin ("ground"). Grid 3 modulates the incoming protons by means of a square-wave voltage which is periodically positive by an amount E_{max} with respect to the vehicle. Grid 2 is at the vehicle potential and serves as an electrostatic shield between the modulating grid and the collector. Grid 1 is maintained about -150 volts with respect to the collector. During the part of the modulating cycle when the voltage on grid 3 is zero (with reference to the vehicle) protons and electrons flow into the cup. The low-energy electrons are repelled by the negative potential on grid 1, but the protons reach the collector. When the modulating voltage is positive and equal to or greater than the energy of the incoming protons, the protons cannot pass grid 3. The electrons are first accelerated and then decelerated by grid 3 and they arrive at and are repelled by grid 1 as before. Thus, there is an AC signal at the collector caused by the alternating arrival of the plasma protons. The photoelectrons from the collector and from grid 1 are not influenced by the modulating voltage because they are shielded from it by grid 2; therefore, the photoelectrons produce a DC (not AC) signal.

The energy of the protons is determined by varying the amplitude of the square-wave modulating voltage E_{max}. For a given value of E_{max}, the AC current to the collector results from those protons with energies less than E_{max}. When the voltage on the positive part of the cycle is less than the proton energy, protons will not be stopped at grid 3, but will arrive at the collector with the same velocity as when the voltage on grid 3 is zero. There will then be no AC signal at the collector. As successively higher modulation voltages are applied, the proton energy is given by that voltage at which the AC signal first appears. This is strictly true, only when the probe is facing in the direction of motion of the plasma. If the protons are incident at an angle Θ to the axis of the probe, the cut-off voltage will be less than that corresponding to the proton energy by a factor $(\cos^2\Theta)$, since the component of the proton velocity in the direction of the field is proportional to $\cos\Theta$. Thus, if Θ is the maximum angle at which protons can enter the cup and reach the collector, the cut-off energy at a given voltage amplitude E_o is $E_o \cos^2\Theta$.

The response of this type of cup has been tested using a small linear accelerator to provide protons of known energy and an ultraviolet source to produce the expected photocurrent. The tests have shown the angular response and energy discrimination to be as expected, and further indicate that no modulation of the photocurrent occurs once outgassing is complete. Laboratory results have been confirmed by the information obtained from Explorer X in which no photoelectric currents were detected when the probe faced the sun.

In addition to the proton measurements described above, this type of probe can also be used to detect electrons. The main problem here is to avoid spurious signals which arise from three sources: (1) modulation of the high-energy electron beam produces a modulated secondary electron current at the collector, (2) any variation of the light intensity incident on the sensor (e.g.,

as a result of vehicle rotation) gives rise to a modulated photoelectric current from various portions of the cup, and (3) photoelectrons produced on the collector side of the modulator grid (predominantly at grid 2) are repelled to the collector during the negative excursion of the modulation voltage and produce a spurious signal.

The first two effects are eliminated by biasing the collector 150 volts positive with respect to a suppressor grid placed at "ground" potential. This is the same method employed to suppress secondary emission and photoelectrons in the proton mode of operation. However, in order to detect electrons of energy less than 100 ev, the potential of the collector and suppressor grid must be interchanged. The third effect (modulation of reverse photocurrent emitted from the shield grid) is minimized by applying a positive voltage of a few hundred volts to a grid placed between the modulating grid and the collector.

B. Mariner A Instrumentation

Since Mariner A is a stabilized vehicle it is necessary to use several sensors to determine the directional properties of the plasma. A minimum of six probes would be required to give complete spherical coverage. Space and weight limitations preclude this number, and as a compromise the experiment utilizes four sensors (faraday cups) with axes 90° apart and lying roughly in the plane of the ecliptic. Each unit covers a solid angle of roughly $2\pi/3$.

The basic measurement cycle is called Data Mode. It consists of separately measuring the proton and electron current to each of the four cups over an energy range from approximately 0 to 2.8 kev. Each measurement gives an "energy window" from $1/3\ E_{max}$ where E_{max} has eight possible values. The values selected (for both protons and electrons) are 2800, 1500, 600, 300, 120, 58, 15, and 7.5 volts. Each set of measurements is made for a boom potential of +25 or −25 volts relative to the spacecraft. Completion of the entire sequence of measurements requires approximately 15 minutes, and it is planned to make eight such measurements per day.

It is likely that there will be periods of high solar activity during which it is desirable to make continuous measurements of the plasma. In order to detect these periods a Monitor Mode of operation is provided in which the outputs of the four cups are placed in parallel and the energy interval accepted is approximately 0 to 3 kev for protons. The output of the cups is sampled at approximately 2.5-minute intervals and if the level exceeds a preset threshold a trigger pulse is sent to the spacecraft Data Automation System. In the Monitor Mode, measurements of the plasma protons are carried out at the maximum possible rate.

The various grid potentials for all five grids of the faraday cups in each of the three equipment operating conditions are given in Table I. The actual programming of the experiment is quite flexible (see the following section on equipment description) and it is possible to start or stop the program at any time.

C. Major Circuits

1. General

The plasma probe instrumentation, a block diagram of which is shown in Fig. 2, consists of three major circuit sections and an ancillary circuit section. The major circuit sections are the measurement link, the high-voltage supply, and the logic. The ancillary circuit section is divided into three groups: (a) boom potential circuits, (b) monitor circuits, and (c) calibration circuits. A brief functional description of each major circuit section, and each ancillary circuit group follows.

2. Measurement Link

The measurement link, which includes the four faraday cups, senses the plasma energy level, processes the signals obtained, and converts the detected signals to a DC analog voltage. The measurement link consists of the following major circuits:

a. Preamplifiers (4)
b. Cup gates (4)
c. Summation amplifier
d. Active twin-T filter
e. Compression amplifier
f. Synchronous detector

a. Preamplifiers

There are four identical preamplifier circuits, one for each faraday cup. Each preamplifier has a closed-loop gain of 20 db. The input signal to each preamplifier is a current within a five-decade range from 10^{-12} to 10^{-7} amp and the output is a 2-kcps square-wave voltage. The preamplifiers have a linear response over a temperature range of −50° to +125°C for the five-decade input signal range.

TABLE I
FARADAY CUP GRID POTENTIALS

Condition	Grid 5	Grid 4	Grid 3	Grid 2	Grid 1	Plate
A Proton measurement (Data Mode)	ground (unit)	ground (unit)	f = 2 kcps v AC +7.5 v thru +2.8 kv 8 steps	ground (unit)	v DC − 100 v in reference to vehicle ground	ground (unit)
B Electron measurement (Data Mode)	ground (unit)	f = 2 kcps v AC −7.5 v thru −2.8 kv 8 steps	v DC + 1000 v	ground (unit)	v DC + 100 v in reference to vehicle ground	ground (unit)
C Proton measurement (Monitor Mode)	ground (unit)	ground (unit)	f = 2 kcps v AC 0 to 3.0 kv (approximately) 1 step	ground (unit)	v DC − 100 v in reference to vehicle ground	ground (unit)

b. Cup Gates

Each preamplifier is followed by a cup gate circuit which performs signal amplification and gating. The gating function selects the particular faraday cup output which will be fed through the measurement link at any given time. The gates are selected and activated in accordance with data from the spacecraft Data Automation System through the instrumentation logic circuits. The cup gate outputs are square-wave signals at 2 kcps which are applied to the summation amplifier.

c. Summation Amplifier

This circuit sums and amplifies the four output signals from the cup gates. The output of the gate summation amplifier is a square-wave signal which is applied to the active twin-T filter.

d. Active Twin-T Filter

The active twin-T filter provides a narrow-band filter (center frequency = 2 kcps) to improve the over-all signal-to-noise characteristics of the measurement link. This output signal is applied to the compression amplifier.

e. Compression Amplifier

The compression amplifier is a logarithmic amplifier covering a five-decade range. The output signal of the compression amplifier is applied to the synchronous detector.

f. Synchronous Detector

The synchronous detector converts the modulated signal from the compression amplifier to a 0- to +6-volt DC analog output signal. This signal is applied to telemetry equipment of the spacecraft.

3. High-Voltage Supply

The high-voltage supply section is divided into five principal circuits.

a. Digital High-Voltage Level Control

The digital high-voltage control receives control signals from the logic circuits in response to program information from the spacecraft Data Automation System. Accordingly, the digital high-voltage level control provides a DC voltage output (1 to 8 levels) to the primary center-tap of the selected high-voltage transformer.

b. Modulator Frequency Generator

The modulator frequency generator produces a 2-kcps output that is applied to the modulator driver circuits and to the calibration circuits.

c. Modulator Driver Circuits

The modulator driver circuits provide a low-impedance source which applies a 2-kcps square-wave signal to the primary of the high-voltage (step-up) transformers.

d. Proton-Electron Selector Circuit

The proton-electron selector circuit consists of relays which operate in response to signals from the logic circuits and route the 2-kcps signal from the modulator driver to the primary of

the selected high-voltage transformer. During Data Mode operation, the 2-kcps signal is applied either to the high-voltage transformer and voltage-doubler combination for the electron modulation grid of the faraday cup, or to the high-voltage transformer and associated voltage-doubler combination for the proton modulation grid of the faraday cup. During Monitor Mode operation, the signal is applied to a third high-voltage transformer and voltage-doubler circuit which covers a range of approximately 0 to 3 kv in one step. This voltage output is applied simultaneously to the proton grids of all four faraday cups.

e. High-Voltage Circuits

The high-voltage circuits contain three transformers, each of which supplies a 2-kcps square-wave voltage (after a single stage of voltage doubling) to either grid 3 (proton) or grid 4 (electron) of the four faraday cups. The modulation voltage level is determined by the voltage level at the center tap (primary) of each transformer. This level is established by the digital high-voltage level control circuits.

4. Logic Circuits

The logic circuits convert the data signals from the spacecraft Data Automation System to binary outputs which are used to control the operation of the equipment. Operational details of the logic circuits are given in later sections of this report.

5. Ancillary Circuits

a. Boom-Potential Circuits

The boom-potential circuits alter the reference potential between the plasma probe unit and the spacecraft body according to the measurements being made. When electron measurements are being made, the plasma probe unit is at a positive potential with respect to the spacecraft; during proton measurements it is at a negative potential.

b. Monitor Circuits

During the Monitor Mode all four cup gates are activated, and proton measurements are made at an energy level corresponding to approximately 0 to 2800 volts. The synchronous detector output level is compared with a reference voltage and when this reference voltage is exceeded, a signal is sent to the ground command station via the Data Automation System. The ground station personnel may then change equipment operation to the Data Mode or allow it to continue in the Monitor Mode, as they desire. The remainder of the measurement link circuits function normally during the Monitor Mode operation.

c. Calibration Circuits

The calibration circuits test the operation of the measurement link circuits. To accomplish this test, signals are applied to the input of the measurement link to verify that the circuits are operating normally. The modulation frequency, high-voltage levels, and the plasma probe ambient temperature are also monitored.

III. EQUIPMENT DESCRIPTION

A. General

As discussed in the preceding sections, the plasma probe provides a means of detecting and measuring particle-number density and energy spectra of interplanetary plasma. The circuits which perform the measurement functions, and which program and control the measurement sequence are described in this section.

B. Measurement Link

The measurement link (see Sec. II-C-2) contains the circuits required to amplify, sum, compress, detect, and convert to a DC analog signal, the 2-kcps plasma signal received from the faraday cups. The DC analog signal has a dynamic range of five decades relative to the faraday cup plasma current range of 10^{-7} to 10^{-12} amp. The 2-kcps signal frequency in the measurement link circuits is derived from the modulator frequency generator (in the high-voltage supply circuits) and represents the rate at which potentials are applied to the faraday cup grids by the high-voltage circuits. Consequently, the plasma current from the cups is modulated at a 2-kcps rate. The 2-kcps signal is detected in the synchronous detector by combining it with the 2-kcps frequency developed in the modulator frequency generator. Figure 3 is a general block diagram of the measurement link.

1. Preamplifier

The measurement link contains four identical preamplifiers, one for each faraday cup. Each preamplifier receives a modulated current signal from its associated faraday cup, amplifies it, and applies it to the related cup gate circuit. The smallest detectable plasma current from the cups is 10^{-12} amp.

A simplified schematic diagram of the preamplifier circuit is given in Fig. 4. The first stage of the preamplifier is a low-noise electrometer tube (CK5886) biased for Class A operation. The anode potential is approximately 9.5 volts and the quiescent anode current is 45 μa. A voltage gain of approximately 17 is obtained from this stage.

The preamplifier has an open-loop gain of 48 db and a closed-loop gain of 20 db. For the maximum input signal (10^{-7} amp at 2 kcps) the output voltage of the preamplifier driving a 24-kohm load is 1 volt peak-to-peak. Equation (1) gives the transfer impedance of the preamplifier circuit shown in Fig. 5,

$$\frac{e_o}{i_s} = \frac{AR_sR_f}{R_f + R_s(1-A)} \approx \frac{AR_s}{1 + \frac{R_s}{R_f}(1-A)} \quad , \tag{1}$$

where

e_o = output signal voltage

i_s = input signal current

R_s = source impedance

R_f = feedback impedance

R_L = load impedance

A = forward gain.

Since $A \gg 1$, then

$$e_o = \frac{AR_s}{1 - \frac{AR_s}{R_f}} i_s \quad . \tag{2}$$

To ensure stability, stabilizing networks have been placed in the anode circuit of the electrometer tube and in the last amplifying state of the preamplifier. The frequency response of the preamplifier is shown in Fig. 6.

The preamplifier operates in the range from 10^{-12} to 10^{-7} amp over an ambient temperature of from $-50°$ to $+125°C$. The output of the preamplifier is applied to the associated cup gate circuit which is now described.

2. Cup Gates

A simplified schematic diagram of one cup gate circuit and the summation amplifier is given in Fig. 7. The outputs of all four cup gates are applied to the summation amplifier when they are gated "on." Since all cup gates are identical, the following description applies to each.

The cup gate circuit consists of two transistors, Q5 and Q6. Q5 is a capacitively coupled common-emitter Class A amplifier. Q6 is located in the emitter circuit of Q5 and operates as a digital switch to provide a gating function. A selected cup preamplifier signal is measured at the correct time by applying a gate signal to the base of Q6. The base of Q5 is biased at 6.0 volts and receives a 2-kcps signal of 10^{-5} to 1 volt peak-to-peak (from the preamplifier). A 3-volt gate signal applied to the base of Q6 will cause this stage to saturate and its collector assumes ground potential, grounding the emitter of Q5. Under these conditions the 2-kcps signal is amplified (Q5 has a voltage gain of 2) and applied to the summation amplifier. When the gate signal at the base of Q6 is zero, the collector of Q6 (and the emitter of Q5) becomes floating and has a high impedance to ground. This shuts off Q5 and isolates the signal, preventing its application to the summation amplifier. The degree of isolation is a function of internal capacitance between the base and collector of Q5 and is approximately 80 db.

When the plasma probe is operated in the Data Mode, the four cup gates are switched sequentially, and the output of each gate is applied to the summation amplifier in turn. In the Monitor Mode, all four cup gates are switched "on" simultaneously and the four outputs are summed in the summation amplifier.

3. Summation Amplifier

The summation amplifier receives a signal from one of the four cup gate circuits (Data Mode), or from all four cup gates (Monitor Mode), amplifies it, and provides a low-impedance drive to the active twin-T filter (see Fig. 7). In order to describe its operation, the summation amplifier portion of Fig. 7 (Q7 and Q8) is redrawn as shown in Fig. 8.

If the amplifier input resistance (R_a) is small compared to the source resistance (R_s), then

$$I_s \approx \frac{e_1}{R} + \frac{e_2}{R} + \frac{e_3}{R} + \frac{e_4}{R} = \frac{1}{R} \sum_{n=1}^{4} e_n \quad . \tag{3}$$

An analysis of the network shows that

$$R_a = \frac{e_i}{I_s} = \frac{R_i}{1 + \frac{R_i}{R_f}(1 + A)} \tag{4}$$

$$\frac{e_o}{I_s} = \frac{Ae_i}{I_s} = \frac{AR_i}{1 + \frac{R_i}{R_f}(1 + A)} \quad . \tag{5}$$

Therefore

$$e_o = \frac{AR_i}{1 + \frac{R_i}{R_f}(1 + A)} \cdot \frac{1}{R} \sum_{n=1}^{4} e_n \quad , \tag{6}$$

where

e_o = output signal voltage

e_1, e_2, e_3, e_4 = input signal voltages

R = adder resistors

R_i = input resistance of grounded emitter amplifier

$$\left(r_b + \frac{r_e}{1 - \alpha_o}\right)$$

A = open-loop voltage gain (Q7 and Q8) .

Numerical quantities associated with Fig. 7, the simplified schematic diagram of the summation amplifier, are as follows. The collector of Q7 is biased (quiescently) at 6.2 volts and the base current is approximately 30 μa. Q7 has a voltage gain of approximately 130. The emitter-follower stage (Q8) is coupled to Q7 by a Zener diode (nominal rating 4.5 volts at 0.4 ma). The voltage drop from the collector of Q7 through the Zener diode biases the base of Q8 at 1.7 volts. The emitter of Q8 is at a 1-volt potential and provides a low-impedance source to drive the active twin-T filter.

4. Active Twin-T Filter

A schematic diagram of the active twin-T filter is shown in Fig. 9. Briefly, the circuit consists of amplifying stages Q8, Q9, and Q10 with the twin-T filter in a negative feedback loop containing amplifiers Q12 and Q11. The filter network provides an amplifier bandwidth of 400 cps (at 2 kcps) and effectively reduces noise from the preamplifier, permitting amplification and detection of small signals in the region $<10^{-10}$ amp.

Figure 10 is a functional block diagram of the active twin-T filter circuit, the operation of which is described in the following paragraphs.

One of the experiments aboard the spacecraft utilizes an extremely sensitive magnetometer capable of measuring fields as low as 10^{-5} gauss. Because of the necessary iron content it is not desirable to use a lumped element LC filter. For this reason an active twin-T filter of the following form was used.

In Fig. 10,

$$A'(s) = \frac{E_o(s)}{E_{in}(s)} = \frac{A(s)}{1 + \beta(s)\, A(s)} \quad . \tag{7}$$

For the purpose of the filter, A(s) is independent of frequency, $A(s) = A_o$, and (s) is a "null" type of frequency sensitive network. Thus, at some frequency $s_o = \omega_o$, $\beta(s_o) = 0$, and the gain becomes

$$A'(s) = \frac{A_o}{1 + \beta(s_o)\, A_o} = A_o \quad . \tag{8}$$

The feedback term $\beta(s)$ is in the form

$$\beta(s) = \beta_o \frac{P(s)}{Q(s)} \quad ,$$

where P(s) and Q(s) are polynomials in s and β_o is given constant. Thus, it can be seen that at frequencies other than f_o, if the product $\beta(s)\, A_o$ is large compared to unity, the gain becomes

$$A' = \frac{A_o}{1 + \beta(s)\, A_o} = \frac{1}{\beta(s)} = \frac{Q(s)}{\beta_o P(s)} \quad . \tag{9}$$

For "twin-T" networks, the degrees of P(s) and Q(s) are the same and thus the filter will have a far frequency attenuation of $1/\beta_o$. Then, since at the center frequency $P(s_o)/Q(s_o) = 0$, the "sharpness" of the filter can be adjusted by adjusting β_o.

For a "twin-T," shown in Fig. 11, the response is

$$H(s) = \frac{E_2(s)}{E_1(s)} = \frac{1 + (4t^2)\, S^2}{1 + (8t)\, S + (4t^2)\, S^2} = \frac{P(s)}{Q(s)} \quad , \tag{10}$$

where t = RC.

The "twin-T" null frequency, which is the filter center frequency, is at

$$\omega_o = \frac{1}{2RC} \quad . \tag{11}$$

The response of the "twin-T" equation [Eq. (10)] assumes an infinite load. A noninfinite load will lower the response H(s) in magnitude but will not affect the presence or location of the null.

In regard to stability, when s is replaced by $j\omega$, Eq. (1) becomes

$$H(j\omega) = \frac{1 - 4t^2\omega^2}{(1 - 4t^2\omega^2) + j(8t\omega)} = \frac{a}{a + jb} \quad . \tag{12}$$

Thus, the angle contributed by an exact "twin-T" can never be greater than 90°. If the rest of the filter circuit (β_o and A_o) has no greater phase shift around the null frequency of the "twin-T," then there will be only the usual high and low cutoff-frequency stability problems. These occur well above and below the frequencies where the "twin-T" contributes any phase shift. However, if the elements within the "twin-T" are not exact in value, there will be no exact "zero" null. Applying the Nyquist criterion, the circle represented by Eq. (8) in the s-plane can be shifted to the left along the t-axis by proper selection of components. Then the loop gain can encircle the $-1 + j0$ point if either β_o of A_o is too high. The result will, of course, be instability. In any result, if the circle does not pass through the origin, the center-frequency filter gain will

not reduce to A_o and will be either larger or smaller depending on the location of the circle. Figure 12 shows the response of a typical filter centered at 2 kcps.

5. Compression Amplifier

The compression amplifier described here, together with the synchronous detector of Sec. III-B-6, serves to compress the wide dynamic range (5 decades) 2-kcps signal from the active twin-T filter into a zero-to-six-volt range DC signal. See Fig. 13.

A compromise was made in selecting the number of amplifiers required to cover the given (80-db) dynamic range. A small number of stages will not reproduce the logarithmic curve accurately and the required gain per stage is high. A large number of stages will define a logarithmic response as accurately as desired. The gain per stage will lower and the number of components will have increased. The compression amplifier used here has seven amplifying stages, each with a (voltage) gain of 4 (12 db) for a total gain of 84 db. Associated with each amplifier stage is a summing resistor and an emitter-follower which drives the following stage.

Under quiescent conditions the collector of each amplifying stage is biased for Class A operation. When a sinusoidal signal of less than 0.7 volt (peak-to-peak) is applied to the base circuit of any amplifying stage, that stage will amplify the signal linearly. Signals greater than 0.7 volt peak-to-peak are limited to this value by the diode network shown in Fig. 14 and produce a constant output.

Figure 15 is a signal-flow diagram of the signal phases from the input to the output of the compression amplifier. The positive-phase signals (a + c = +1 and e + g = +3), after the indicated amplifying stage a, c, e, and g, are summed to give a positive-phase signal (1 + 3). The negative-phase signals (b + d = −2 and f + h = −4), after the indicated amplifying stage b, d, f, and h, are summed to give a negative-phase signal [−2 + (−4)]. Summing both positive- and negative-phase signals yields the total compressed signal, i.e., summing (1 + 2 + 3 + 4).

When a signal potential of 0.5×10^{-3} volts peak-to-peak is applied to the compression amplifier, each of the seven stages (b through h, Fig. 13) will amplify the signal by a gain of 12 db (only stage h will be in a limited condition). Increasing the signal magnitude by four decades (in single decade steps) will sequentially place stages e, d, c, and b in a limited condition.

The signals from each amplifying stage are summed by taking the signal from each amplifying point of similar phase polarity through a resistor adder network and feeding it to the emitter of a common-base amplifier as shown in Fig. 16. The collectors of all common-base amplifiers are connected to the primaries of a balanced-to-unbalanced transformer. The combined positive-phase signals (1 and 3, Figs. 15 and 16) are summed at one end of the transformer primary through two common-base stages (Q15 and Q16) while combined negative-phase signals (2 and 4) are summed at the opposite end of the transformer primary through two common-base stages (Q17 and Q18). The net result is the summing of all signals leaving the eight signal points of the compression amplifier. The output signal level from the compression amplifier summing circuit is controlled by adjusting the load across the secondary of the summing transformer. Figure 17 gives the transfer characteristics of this compression amplifier.

6. Synchronous Detector

The synchronous detector converts the compressed 2-kcps signal from the compression amplifier into a DC output having a range of 0 to +6 volts. A simplified schematic diagram of the synchronous detector is given in Fig. 18.

Basically, the synchronous detector is a diode-bridge ring-demodulator. The 2-kcps input signal from the compression amplifier is demodulated by mixing it with a 2-kcps carrier signal from the modulator frequency generator. The output contains a DC and a 4-kcps component (twice the operating frequency). The output amplitude is a function of the amplitude of the input signal and the phase difference between the input signal and the carrier signal. The 4-kcps component is eliminated by a low-pass filter at the detector output. The DC term at the output depends on the amplitude of the input signal and the phase difference between the input signal and the carrier signal.

The signal from the compression amplifier summing circuit is applied to the secondary center tap of the synchronous detector transformer. The carrier signal from the modulator drive circuit is applied to the transformer primary and causes the two diode sets to conduct alternately at the 2-kcps rate. In the absence of the compression amplifier signal the output of the synchronous detector is zero because of the balanced arrangement of the diodes. During the time a signal from the summing circuit is present, the signal current flows through the "on" diode set and charges the associated capacitor.

The 2-kcps modulator drive applied to the synchronous transformer alternately opens and closes the diode sets allowing the signal current to charge the capacitors. If the signal current is in phase with the modulator drive, the positive signal excursions charge the capacitor associated with the "on" diode set during this time interval, then the negative signal excursions charge the alternate capacitor through the second diode set during the negative time interval with a polarity that adds to the charge of the first capacitor. The total charge of the two capacitors is taken as the output voltage and its polarity is dependent on the exact phasing of the modulator drive and compression amplifier signal.

For the case of unequal signal and modulator drive frequencies, the accumulated charge on the capacitors resulting from the signal is zero. Detection is possible only when signal and modulator drive frequencies are exactly equal. Figure 19 is an analog plot of preamplifier input current vs synchronous detector output voltage.

C. High-Voltage Supply Circuits

The following paragraphs describe the arrangement and function of the major high-voltage supply circuits. A simplified schematic diagram of each circuit is provided.

1. Modulator Frequency Generator

The modulator frequency generator (Fig. 20) is a basic timing source which produces a 2-kcps square wave. The square wave is used as the modulating frequency for the high-voltage circuits, the carrier frequency for the synchronous detector, and as a calibration signal during the calibrate phase of the Data Mode operation. The circuit sections which comprise the modulator frequency generator are now described.

a. Astable Multivibrator

The astable multivibrator produces a 4-kcps output frequency which is converted to 2 kcps by the commutating flip-flop circuit. To limit frequency drift to an acceptable 2 percent over a temperature range of $-20°$ to $+100°C$, special low-temperature-coefficient capacitors are employed in the timing circuit. This degree of frequency stability is set by the bandwidth of the

active twin-T filter in the measurement link. A change in the filter center-frequency (caused by frequency drift) will reduce the output level from the filter.

b. Commutating Flip-Flop

The commutating flip-flop is a conventional (transistorized) binary circuit. It is triggered by a negative pulse developed from the trailing edge of the 4-kcps astable multivibrator pulse. Emitter-followers in each collector circuit provide a low impedance source to drive the modulator driver circuit which follows the modulator frequency generator.

c. Gate Circuit

The duty cycle of the modulator frequency generator is controlled by a signal from the logic circuits. This "duty cycle gate" is a +3-volt signal of one-second duration which is applied to the base of "gate transistor" Q20 and causes it to saturate. Q21 is in series with Q20 and also saturates, providing a 4-kcps signal is present from the astable multivibrator.

In the event that the multivibrator fails, Q21 loses its base voltage and becomes unsaturated, raising the emitter voltage of the flip-flop to +6 volts. Raising the emitters results in a positive voltage at both transistor collectors in the flip-flop, preventing large currents in the driver section.

Under these conditions the emitters of Q22 and Q23, which constitute the commutating flip-flop, are returned to ground. If either Q21 or Q20 are "off," the bias conditions at Q22 and Q23 are chosen so that the 4-kcps signal from the multivibrator will not initiate operation of the commutating flip-flop. Q22 and Q23 are coupled to the modulator driver via the emitter followers.

2. Modulator Driver Circuit

The modulator driver circuit (Fig. 21) consists of a chopper which supplies a variable square-wave voltage to the primaries of the high-voltage transformers in the high-voltage circuits. The modulator driver is supplied with a variable DC voltage from the high-voltage level control circuit (see Sec. III-C-5). The chopping frequency is controlled by a signal from the modulator frequency generator. After chopping, the resulting 2-kcps square-wave signal is applied to the primary of one of the three step-up high-voltage transformers in the high-voltage circuit by relays in the high-voltage selector circuit.

When a chopped signal at point A is negative (3 volts), Q30 is turned "on" with a base drive current of approximately 1 ma. The collector current of Q30 provides the base drive for Q31 which drives one-half of the center-tapped transformer primary. When point A is negative, point B is positive (3 volts) and the base of Q32 is cut off and no current flows in the second half of the center-tapped transformer primary.

During chopper operation the voltage applied to each half-primary is determined by the digital high-voltage level control. Primary voltage from this circuit is applied between the transformer center-tap and ground with the chopper serving as an electronic switch, applying voltage alternately to each half-primary at the timing frequency rate (2 kcps).

3. High-Voltage Circuits

The high-voltage circuits consist of the three high-voltage transformers (Fig. 21) and three diode voltage-doubling rectifiers. The functions of these major circuits are now described.

a. High-Voltage Transformers

Three high-voltage transformers, each driving a diode voltage-doubling rectifier circuit, supply the grid potentials to the faraday cups for the Data Mode and the Monitor Mode measurements. The proper transformer for a particular measurement is selected by relays in the high-voltage selector section. Primary voltage applied to the selected transformer from the modulator driver circuit is provided in eight progressive levels by the regulator circuit in the digital high-voltage level control. The sequence of grid potential application to the four faraday cups is determined by the digital high-voltage level control. Transformer secondary voltage, prior to doubling, ranges from 3.75 volts to approximately 2000 volts peak-to-peak in eight discrete levels. Maximum transformer secondary voltage is obtained with approximately 56 volts peak-to-peak applied to each half-primary. At this maximum level approximately 70 ma is supplied to the transformer primary from the regulator circuit in the digital high-voltage level control.

b. Modulator Driver Supplies

Simplified schematic diagrams of the positive and negative high-voltage supplies are shown in Fig. 22(a) and (b), respectively. Each supply consists of a half-wave rectifier and DC level shifter; the negative and positive supplies are identical except for inversion of the diodes. At the highest modulation level, the circuit shown in Fig. 22(a) operates as follows. The output of the transformer is a square wave of approximately ±1000 volts; CR1 conducts during the positive-voltage excursion and C1 becomes charged to +1000 volts. This voltage also appears at the output side of C2 because CR2 prevents the output voltage from going negative with respect to the potential of C1. The full voltage variation at the transformer output is coupled to the output of C2 so that the net result is approximately a 2-kv square wave superimposed on a 1-kv DC level.

Figure 23 is a graphical representation of the measured voltage levels for the positive modulator. A −6-volt bias indicated in Fig. 22 shifts the voltage levels so that the lowest step actually goes negative (see Sec. IV-C-1-a). The level sequence for the electron mode is similar.

It can be shown that the power supplied by the modulator is approximately

$$P = fC(\Delta V)^2 \quad ,$$

where

f = modulator frequency

C = total load capacitance

ΔV = square wave peak-to-peak value (DC level omitted) .

If f = 2 kcps, C = 240 pf, and $\Delta V \cong$ 1800 volts (the highest possible value), the calculated power to the load is 1.6 watts while the input power required by the high-voltage driver and regulator is 3.9 watts.

4. High-Voltage Selector Circuit

The high-voltage selector circuit consists of selector relays I and II and the related relay drivers (see Fig. 21). The high-voltage selector circuit selects and energizes one of the three high-voltage transformers in response to command signals from the logic circuit. A different transformer is selected for each phase and mode of measurement.

a. Selector Relays

Selector relays I and II operate in the sequence given in the table of Fig. 21. For a selected measurement and mode of operation, the relay contacts complete the primary circuit between the proper high-voltage transformer and the regulator supply (through the modulator driver circuit). Individual relay drivers operate relays I and II as shown in Fig. 21; the driver circuits are identical.

b. Relay Drivers

The relay driver circuit shown in Fig. 21 operates in the following manner. When a step function signal from the logic circuit (+3 volts) is applied to the base of Q40, the collector drops to approximately ground potential. The collector of Q40 drives the complementary emitter-follower Q41. Q41 is biased "off" which biases Q42 "on," discharging capacitor C1 and de-energizing relay I. When the +3-volt signal is removed from the base of Q40 the collector potential increases to approximately +12 volts. This biases the complementary emitter-follower Q41 "on" (and Q42 "off") permitting the current from Q41 to charge C1 and energize relay I. A network formed by C1 and R1 (in series with the relay coil) permits the relay to respond to a step function.

5. Digital High-Voltage Level Control

The digital high-voltage level control (see Fig. 24) consists of a digital gate circuit, current supply circuits, and a regulator circuit. The digital high-voltage level control supplies and controls primary voltage levels applied to the selected high-voltage transformer (see Sec. III-C-4). Eight sequential voltage levels from the high-voltage transformer secondary (shown in Fig. 23) are applied to the four faraday cups during the Data Mode measurements. Operation of the digital high-voltage level control circuit is controlled by digital signals from the logic circuits.

a. Digital Gates

The digital gates and the current supply circuits which they control are shown in Fig. 24. The digital gates consist of seven identical stages (the Q23 row) with each stage controlling one of seven identical (except for resistor values) current regulator stages (the Q22 row). Each digital gate is a common-emitter transistor normally biased "off" so that the collector current is zero. When a +3-volt signal from the logic circuit is applied to the base of a given gate, that transistor stage is biased "on," collector current flows, and the collector assumes a ground potential. For example, if a +3-volt signal is applied to the base of Q23, the collector (which is at ground potential) effectively grounds resistor R1. This circuit action permits base current to flow in Q22, producing a rise in collector current and saturating Q22. Collector voltage increases to approximately 12 volts. Q22 (when saturated) operates as a voltage source across resistor R2 and produces a current flow determined by the collector voltage and the value of R2. Each digital gate operates in this manner and controls the associated current supply stage.

b. Current Supply Circuit

The current supply circuit (row Q22 in Fig. 24) consists of seven identical stages. Each stage is controlled by the associated digital gate stage (row Q23 in Fig. 24). When each current supply stage is biased "on" by the related digital gate stage, the collector voltage rises to

approximately 12 volts. The value of collector resistor R2 is different at each stage. Consequently, summing stage Q24 receives different current levels which are determined by the collector saturation voltage and the value of R2 at each stage. Summing stage Q24 controls the output level from the regulator circuit and ultimately the mode-measurement voltage level produced by the high-voltage transformers in the high-voltage circuits.

To obtain selectable voltage increments from the high-voltage transformers, similar current increments must be produced by the regulator circuit. Each increment (from one to eight) has an equal logarithmic voltage relation determined by the value of resistor R2 in each of the current supply stages. The value of R2 is determined in the following manner.

The value of resistor R2 for the first current supply stage is established as 1.8 kohm to produce a collector current of approximately 3 ma at summing stage Q24. This value of summing current, by controlling the regulator circuit, produces a maximum potential of approximately 2800 volts at the modulating grid of the four faraday cups. The value of the remaining current-determining resistors (R2) for the other current supply stages is increased by a factor of 2.1 (relative to the initial 1.8-kohm value) to obtain an equal logarithmic voltage relation as shown in Fig. 23.

c. Regulator Circuit

The regulator circuit (see Fig. 24) operates as follows. A predetermined current of 6 ma is applied to the emitters of Q20 and Q27. The relative amount of the 6 ma which flows into Q20 is determined by the amount of collector current from Q24, which is in turn determined by the current supply gates. The remaining portion flows in Q27.

For the case of the lowest collector current from Q24, almost all of the 6 ma will flow into Q27. This leaves a small drive current in Q20, and consequently in Q25 and Q26, which results in a minimum voltage level at the output of Q26. As the collector current in Q24 increases, less base current is allowed in Q28 and Q27, and a greater portion of the 6-ma current flows into the emitter of Q20. This increased emitter current in Q20 results in larger output drive currents in Q25 and Q26.

The collector current from Q24 effectively causes a current balance so that a fixed amount of the 6-ma current flows into Q27. The remaining portion, which flows into Q20, ultimately determines the output drive and voltage level. The feedback resistor R3 establishes the current balance, and senses any variation in output level once it is established, and regulates the output voltage by readjusting the base current of Q28.

D. Logic Circuit Operation

The logic circuits control the operation of the cup gates, the high-voltage supply circuit, the boom potential circuit, and the monitor circuit. Data Automation System signals received by the spacecraft are applied to the logic circuits and processed to produce digital control signals which program the plasma probe experiment. Operation of the faraday cups and the cup gates is controlled to obtain proton and electron plasma measurements at eight incremental levels from each of the four faraday cups. There are two major measurement modes: the Data Mode and the Monitor Mode. A description of each mode is given in the following paragraphs. A simplified block diagram of the logic circuits is given in Fig. 25.

1. Data Mode

The Data Mode consists of three measurement phases: proton measurements, electron measurements, and an internal calibration phase. During the proton measurement phase, plasma protons are detected and measured in response to programmed signals from the Data Automation System. A particular faraday cup is selected and eight values of grid voltage are applied in incremental steps. A total of 64 measurements are performed during this phase. Eight increments are applied to each of the four faraday cups for each of two potentials between the plasma probe boom and the spacecraft body.

During the electron measurement phase, plasma electrons are detected and measured by the measurement link. The sequence and number of measurements are identical to the proton phase measurements.

A calibration phase which follows the proton and electron measurement phases completes the Data Mode measurements. During calibration, an internal test signal verifies normal operation of the measurement link circuits. In addition, temperature, frequency, and high-voltage measurements are performed. The calibration phase is controlled by programmed signals from the Data Automation System which are converted to digital control signals by the logic circuit. Calibration results are sent to the ground command station and provide continual monitoring of equipment operation.

2. Monitor Mode

The Monitor Mode directly follows the Data Mode and measures plasma protons only. Any one of eight measurement levels may be selected by the ground command as a threshold level. Plasma activity below the selected threshold level will not be measured. The duration of the Monitor Mode may be controlled by the ground station, and the threshold level may be changed at any time during this period. When plasma activity greater than the selected threshold level occurs, a 40-μsec pulse is transmitted to the ground station. When so notified the ground command may change the threshold level, or select a desired Data Mode phase to obtain measurements of proton or electron activity.

3. Mode Programming

To provide the desired sequencing of the operational modes of the experiment with the given command line sequence it is necessary to employ intermediate conversion logic circuits prior to the general logic circuits. Line-serial subprogram information is given in Table II.

A detailed block diagram of the logic circuit is given in Fig. 26. The data automation logic lines are fed to heavy-duty logic buffers to provide isolation and minimum loading of the logic lines. The preliminary diode gates, inverter and multivibrator (OS), and the gates associated with the experiment main logic flip-flops, convert the command pulse sequence to a logic arrangement which provides the proper experiment operation. The command functions are listed in Table III in the order of occurrence. In Table III the experiment operational states are shown under the logic columns for each command function. A complete description of the entire sequence of command function is not possible, but several cases will be considered as examples.

For the first command function listed, one pulse occurs on line 61 and one pulse on line a. The "and" gate circled with a 2 following $\ell 61$ receives both pulses and passes the combined pulses as a reset to all the experiment logic circuits. In the case of the fourth command pulse,

TABLE II

LINE SERIAL INFORMATION
(Mariner A Subprogram Experiment)

	Command	Pulse	State of Binary														Time Tuit* (octal)
			CS_1	CS_0	BP_1	BP_0	PE	ES_2	ES_1	ES_0	MD_1	MD_0	CA_1	CA_0	MV	OS	
Cup 1	ℓ41 · a	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	ℓ44 · a	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1^{Δ}	4
	ℓ45 E1 a	1	0	0	0	0	0	0	0	0	0	0	0	0	1^{Δ}	0	5
	ℓ45 E2	2	0	0	0	0	0	0	0	1^{Δ}	0	0	0	0	1	0	15
	ℓ45 E3	3	0	0	0	0	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	25
	ℓ45 E4	4	0	0	0	0	0	0	1	1^{Δ}	0	0	0	0	1	0	35
Cup 1	ℓ44 3 · b	dead	0	0	0	0	0	0	1	1	0	0	0	0	0^{Δ}	0	44
	ℓ45 E1 b	1	0	0	0	0	0	1^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0	45
	ℓ45 E2	2	0	0	0	0	0	1	0	1^{Δ}	0	0	0	0	1	0	55
	ℓ45 E3	3	0	0	0	0	0	1	1^{Δ}	0^{Δ}	0	0	0	0	1	0	65
	ℓ45 E4	4	0	0	0	0	0	1	1	1^{Δ}	0	0	0	0	1	0	75
Cup 2	ℓ44 · a	2	0	1^{Δ}	0	0	0	1	1	1	0	0	0	0	0^{Δ}	1^{Δ}	104
	ℓ45 E1 a	1	0	1	0	0	0	0^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	105
	ℓ45 E2	2	0	1	0	0	0	0	0	1^{Δ}	0	0	0	0	1	0	115
	E3	3	0	1	0	0	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	125
	E4	4	0	1	0	0	0	0	1	1^{Δ}	0	0	0	0	1	0	135
Cup 2	ℓ44 4b dead	dead	0	1	0	0	0	0	1	1	0	0	0	0	0^{Δ}	0	144
	ℓ45 E1 b	1	0	1	0	0	0	1^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0	145
	E2	2	0	1	0	0	0	1	0	1^{Δ}	0	0	0	0	1	0	155
	E3	3	0	1	0	0	0	1	1^{Δ}	0^{Δ}	0	0	0	0	1	0	165
	E4	4	0	1	0	0	0	1	1	1^{Δ}	0	0	0	0	1	0	175
Cup 3	ℓ44 3 a	3	1^{Δ}	0^{Δ}	0	0	0	1	1	1	0	0	0	0	0^{Δ}	1^{Δ}	204
	ℓ45 E1 a	1	1	0	0	0	0	0^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	205
	E2	2	1	0	0	0	0	0	0	1^{Δ}	0	0	0	0	1	0	215
	E3	3	1	0	0	0	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	225
	E4	4	1	0	0	0	0	0	1	1^{Δ}	0	0	0	0	1	0	235
Cup 3	ℓ44 1 b	dead	1	0	0	0	0	0	1	1	0	0	0	0	0^{Δ}	0	244
	ℓ45 E1 b	1	1	0	0	0	0	1^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0	245
	ℓ45 E2	2	1	0	0	0	0	1	0	1^{Δ}	0	0	0	0	1	0	255
	E3	3	1	0	0	0	0	1	1^{Δ}	0^{Δ}	0	0	0	0	1	0	265
	E4	4	1	0	0	0	0	1	1	1^{Δ}	0	0	0	0	1	0	275
Cup 4	ℓ44 4 a	4	1	1^{Δ}	0	0	0	1	1	1	0	0	0	0	0^{Δ}	1^{Δ}	304
	ℓ45 E1 a	1	1	1	0	0	0	0^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	305
	ℓ45 E2	2	1	1	0	0	0	0	0	1^{Δ}	0	0	0	0	1	0	315
	E3	3	1	1	0	0	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	325
	E4	4	1	1	0	0	0	0	1	1^{Δ}	0	0	0	0	1	0	335

*One tuit equals 660 msec.

TABLE II (Continued)

	Command	Pulse	State of Binary														Time Tuit (octal)
			CS_1	CS_0	BP_1	BP_0	PE	ES_2	ES_1	ES_0	MD_1	MD_0	CA_1	CA_0	MV	OS	
Cup 4	ℓ44 2 b	dead	1	1	0	0	0	0	1	1	0	0	0	0	0^{Δ}	0	344
	ℓ45 E1 b	1	1	1	0	0	0	1^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0	345
	E2	2	1	1	0	0	0	1	0	1^{Δ}	0	0	0	0	1	0	355
	E3	3	1	1	0	0	0	1	1^{Δ}	0^{Δ}	0	0	0	0	1	0	365
	E4	4	1	1	0	0	0	1	1	1^{Δ}	0	0	0	0	1	0	375
Cup 1	ℓ41 · b	1	1	1	1	1	0	1	1	1	0	0	0	0	0	0	401
	ℓ44 1 a	1	0^{Δ}	0^{Δ}	1	1	0	1	1	1	0	0	0	0	0	1^{Δ}	404
	ℓ45 E1 a	1	0	0	1	1	0	0^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	405
	E2	2	0	0	1	1	0	0	0	1^{Δ}	0	0	0	0	1	0	415
	E3	3	0	0	1	1	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	425
	E4	4	0	0	1	1	0	0	1	1^{Δ}	0	0	0	0	1	0	435
Cup 3	ℓ44 3 b	3	1^{Δ}	0	1	1	0	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	444
	ℓ45 E1 b	1	1	0	1	1	0	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	445
	E2	2	1	0	1	1	0	0	0	1^{Δ}	0	0	0	0	1	0	455
	E3	3	1	0	1	1	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	465
	E4	4	1	0	1	1	0	0	1	1^{Δ}	0	0	0	0	1	0	475
Cup 2	ℓ44 2 a	2	0^{Δ}	1^{Δ}	1	1	0	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	504
	ℓ45 E1 a	1	0	1	1	1	0	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	505
	E2	2	0	1	1	1	0	0	0	1^{Δ}	0	0	0	0	1	0	515
	E3	3	0	1	1	1	0	0	1^{Δ}	0^{Δ}	0	0	1	1	1	0	525
	E4	4	0	1	1	1	0	0	1	1^{Δ}	0	0	1	1	1	0	535
Cup 4	ℓ44 4 b	4	1^{Δ}	1	1	1	0	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	544
	ℓ45 E1 b	1	1	1	1	1	0	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	545
	E2	2	1	1	1	1	0	0	0	1^{Δ}	0	0	0	0	1	0	555
	E3	3	1	1	1	1	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	565
	E4	4	1	1	1	1	0	0	1	1^{Δ}	0	0	0	0	1	0	575
Cup 3	ℓ43 1p a	1	1	1	0^{Δ}	1	0	0	1	1	0	0	0	0	0^{Δ}	0	601
	ℓ44 3 a	3	1	0^{Δ}	0	1	0	0	1	1	0	0	0	0	0	1^{Δ}	604
	ℓ45 E1 a	1	1	0	0	1	0	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	605
	E2	2	1	0	0	1	0	0	0	1^{Δ}	0	0	0	0	1	0	615
	E3	3	1	0	0	1	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	625
	E4	4	1	0	0	1	0	0	1	1^{Δ}	0	0	0	0	1	0	635
Cup 1	ℓ44 1 b	1	0^{Δ}	0	0	1	0	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	644
	ℓ45 E1 b	1	0	0	0	1	0	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	645
	E2	2	0	0	0	1	0	0	0	1^{Δ}	0	0	0	0	1	0	655
	E3	3	0	0	0	1	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	665
	E4	4	0	0	0	1	0	0	1	1^{Δ}	0	0	0	0	1	0	675

TABLE II (Continued)

	Command	Pulse	State of Binary														Time Tuit (octal)
			CS_1	CS_0	BP_1	BP_0	PE	ES_2	ES_1	ES_0	MD_1	MD_0	CA_1	CA_0	MV	OS	
Cup 4	ℓ44 4 a	4	1^{Δ}	1^{Δ}	0	1	0	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	704
	ℓ45 E1 a	1	1	1	0	1	0	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	705
	E2	2	1	1	0	1	0	0	0	1^{Δ}	0	0	0	0	1	0	715
	E3	3	1	1	0	1	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	725
	E4	4	1	1	0	1	0	0	1	1^{Δ}	0	0	0	0	1	0	735
Cup 2	ℓ44 2 b	2	0^{Δ}	1	0	1	0	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	744
	ℓ45 E1 b	1	0	1	0	1	0	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	745
	E2	2	0	1	0	1	0	0	0	1^{Δ}	0	0	0	0	1	0	755
	E3	3	0	1	0	1	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	765
	E4	4	0	1	0	1	0	0	1	1^{Δ}	0	0	0	0	1	0	775
Cup 1	ℓ41 N b	1	0	1	0	0	1	0	1	1	0	0	0	0	0	0	1001
	ℓ44 1 a	1	0	0^{Δ}	0	0	1	0	1	1	0	0	0	0	0	1	1004
	ℓ45 E1 a	1	0	0	0	0	1	0	0^{Δ}	0^{Δ}	0	0	0	0	1	0	1005
	E2	2	0	0	0	0	1	0	0	1^{Δ}	0	0	0	0	1	0	1015
	E3	3	0	0	0	0	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1025
	E4	4	0	0	0	0	1	0	1	1^{Δ}	0	0	0	0	1	0	1035
Cup 1	ℓ44 3 b	dead	0	0	0	0	1	0	1	1	0	0	0	0	0	0	1044
	ℓ45 E1 b	1	0	0	0	0	1	1^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1	0	1045
	E2	2	0	0	0	0	1	1	0	1^{Δ}	0	0	0	0	1	0	1055
	E3	3	0	0	0	0	1	1	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1065
	E4	4	0	0	0	0	1	1	1	1^{Δ}	0	0	0	0	1	0	1075
Cup 2	ℓ44 2 a	2	0	1^{Δ}	0	0	1	1	1	1	0	0	0	0	0	1	1104
	ℓ45 E1 a	1	0	1	0	0	1	0^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1	0	1105
	E2	2	0	1	0	0	1	0	0	1^{Δ}	0	0	0	0	1	0	1115
	E3	3	0	1	0	0	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1125
	E4	4	0	1	0	0	1	0	1	1^{Δ}	0	0	0	0	1	0	1135
Cup 2	ℓ44 4 b	dead	0	1	0	0	1	0	1	1	0	0	0	0	0	0	1144
	ℓ45 E1 b	1	0	1	0	0	1	1^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1	0	1145
	E2	2	0	1	0	0	1	1	0	1^{Δ}	0	0	0	0	1	0	1155
	E3	3	0	1	0	0	1	1	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1165
	E4	4	0	1	0	0	1	1	1	1^{Δ}	0	0	0	0	1	0	1175
Cup 3	ℓ44 a	3	1^{Δ}	0^{Δ}	0	0	1	1	1	1	0	0	0	0	0	1	1204
	ℓ45 E1 a	1	1	0	0	0	1	0^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1	0	1205
	E2	2	1	0	0	0	1	0	0	1^{Δ}	0	0	0	0	1	0	1215
	E3	3	1	0	0	0	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1225
	E4	4	1	0	0	0	1	0	1	1^{Δ}	0	0	0	0	1	0	1235
Cup 3	ℓ44 1 b	dead	1	0	0	0	1	0	1	1	0	0	0	0	0	0	1244
	ℓ45 E1 b	1	1	0	0	0	1	1^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1	0	1245
	E2	2	1	0	0	0	1	1	0	1^{Δ}	0	0	0	0	1	0	1255
	E3	3	1	0	0	0	1	1	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1265
	E4	4	1	0	0	0	1	1	1	1^{Δ}	0	0	0	0	1	0	1275

TABLE II (Continued)

	Command	Pulse	State of Binary														Time Tuit (octal)
			CS_1	CS_0	BP_1	BP_0	PE	ES_2	ES_1	ES_0	MD_1	MD_0	CA_1	CA_0	MV	OS	
Cup 4	ℓ44 4 a	4	1	1^{Δ}	0	0	1	1	1	1	0	0	0	0	0	1	1304
	ℓ45 E1 a	1	1	1	0	0	1	0^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1	0	1305
	E2	2	1	1	0	0	1	0	0	1^{Δ}	0	0	0	0	1	0	1315
	E3	3	1	1	0	0	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1325
	E4	4	1	1	0	0	1	0	1	1^{Δ}	0	0	0	0	1	0	1335
	ℓ44 2 b	dead	1	1	0	0	1	0	1	1	0	0	0	0	0	0	1344
	ℓ45 E1 b	1	1	1	0	0	1	1^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1	0	1345
	E2	2	1	1	0	0	1	1	0	1^{Δ}	0	0	0	0	1	0	1355
	E3	3	1	1	0	0	1	1	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1365
	E4	4	1	1	0	0	1	1	1	1^{Δ}	0	0	0	0	1	0	1375
	ℓ41 b	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1401
	ℓ44 1 a	1	0^{Δ}	0^{Δ}	1	1	1	1	1	1	0	0	0	0	0	1^{Δ}	1404
	ℓ45 E1 a	1	0	0	1	1	1	0^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0	1405
	E2	2	0	0	1	1	1	0	0	1^{Δ}	0	0	0	0	1	0	1415
	E3	3	0	0	1	1	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1425
	E4	4	0	0	1	1	1	0	1	1^{Δ}	0	0	0	0	1	0	1435
	ℓ44 3 b	3	1^{Δ}	0	1	1	1	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	1444
	ℓ45 E1 b	1	1	0	1	1	1	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0	1445
	E2	2	1	0	1	1	1	0	0	1^{Δ}	0	0	0	0	1	0	1455
	E3	3	1	0	1	1	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1465
	E4	4	1	0	1	1	1	0	1	1^{Δ}	0	0	0	0	1	0	1475
	ℓ44 2 a	2	0^{Δ}	1^{Δ}	1	1	1	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	1504
	ℓ45 E1 a	1	0	1	1	1	1	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	1505
	E2	2	0	1	1	1	1	0	0	1^{Δ}	0	0	0	0	1	0	1515
	E3	3	0	1	1	1	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1525
	E4	4	0	1	1	1	1	0	1	1^{Δ}	0	0	0	0	1	0	1535
	ℓ44 4 b	4	1^{Δ}	1	1	1	1	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	1544
	ℓ45 E1 b	1	1	1	1	1	1	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	1545
	E2	2	1	1	1	1	1	0	0	1^{Δ}	0	0	0	0	1	0	1555
	E3	3	1	1	1	1	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1565
	E4	4	1	1	1	1	1	0	1	1^{Δ}	0	0	0	0	1	0	1575
	ℓ43 a	1	1	1	0^{Δ}	1	1	0	1	1	0	0	0	0	0	0	1601
	ℓ44 3 a	3	1	0^{Δ}	0	1	1	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	1604
	ℓ45 E1 a	1	1	0	0	1	1	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	1605
	E2	2	1	0	0	1	1	0	0	1^{Δ}	0	0	0	0	1	0	1615
	E3	3	1	0	0	1	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1625
	E4	4	1	0	0	1	1	0	1	1^{Δ}	0	0	0	0	1	0	1635

Cup 4 Pulse

TABLE II (Continued)

Command	Pulse	State of Binary														Time Tuit (octal)
		CS_1	CS_0	BP_1	BP_0	PE	ES_2	ES_1	ES_0	MD_1	MD_0	CA_1	CA_0	MV	OS	
ℓ44 1 b	1	0^{Δ}	0	0	1	1	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	1644
ℓ45 E1 b	1	0	0	0	1	1	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	1645
E2	2	0	0	0	1	1	0	0	1^{Δ}	0	0	0	0	1	0	1655
E3	3	0	0	0	1	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1665
E4	4	0	0	0	1	1	0	1	1^{Δ}	0	0	0	0	1	0	1675
ℓ44 a	4	1^{Δ}	1^{Δ}	0	1	1	0	1	1	0	0	0	0	0^{Δ}	1^{Δ}	1704
ℓ45 E1 a	1	1	1	0	1	1	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	1705
E2	2	1	1	0	1	1	0	0	1^{Δ}	0	0	0	0	1	0	1715
E3	3	1	1	0	1	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1725
E4	4	1	1	0	1	1	0	1	1^{Δ}	0	0	0	0	1	0	1735
ℓ44 2 b	2	0^{Δ}	1	0	1	1	0	1	1	0	0	0	0	0^{Δ}	1	1744
ℓ45 E1 b	1	0	1	0	1	1	0	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0^{Δ}	1745
E2	2	0	1	0	1	1	0	0	1^{Δ}	0	0	0	0	1	0	1755
E3	3	0	1	0	1	1	0	1^{Δ}	0^{Δ}	0	0	0	0	1	0	1765
E4	4	0	1	0	1	1	0	1	1^{Δ}	0	0	0	0	1	0	1775
ℓ43 b	1	0	1	0	0^{Δ}	0^{Δ}	0	1	1	0	1^{Δ}	0	0	0^{Δ}	0	1777
46 b	1	0	1	0	0	0	0	0^{Δ}	0^{Δ}	0	1	0	0	1^{Δ}	0	1777+
46 a	1	0	1	0	0	0	0	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1777+
	1	0	1	0	0	0	0	0	0	1	0	0	1^{Δ}	0	0	
	1	0	1	0	0	0	0	0	0	1	0	1^{Δ}	0^{Δ}	0	0	
	1	0	1	0	0	0	0	0	0	1	0	1	1^{Δ}	0	0	

TABLE III

COMMAND FUNCTIONS

Command Lines	Pulse No. 40 μsec	Function	Binary State												
			CS_1	CS_0	BP_1	PE	ES_2	ES_1	ES_0	MD_1	MD_0	CA_1	CA_0	MV	OS
61 a 5A	1	Sets Data Mode Proton measurement Boom −25 volts (DC)	0	0	0	0	0	0	0	0	0	0	0	0	0
60 a En	1	Select 1 energy level	0	0	0	0	0	0	0	0	0	0	0	1^{Δ}	0
60 a En	2	Select 2 energy level	0	0	0	0	0	0	1^{Δ}	0	0	0	0	1^{Δ}	0
60 a En	3	Select 3 energy level	0	0	0	0	0	1^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0
60 a En	4	Select 4 energy level	0	0	0	0	0	1^{Δ}	1^{Δ}	0	0	0	0	1^{Δ}	0
60 b En	1	Select 5 energy level	0	0	0	0	1^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0
60 b En	2	Select 6 energy level	0	0	0	0	1	0	1^{Δ}	0	0	0	0	1^{Δ}	0
60 b En	3	Select 7 energy level	0	0	0	0	1	1^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0
60 b En	4	Select 8 energy level	0	0	0	0	1	1	1^{Δ}	0	0	0	0	1^{Δ}	0
60 d En	1	Select 1 energy level	0	0	0	0	0^{Δ}	0^{Δ}	0^{Δ}	0	0	0	0	1^{Δ}	0
70 a An	1	Select cup 1	0	0	0	0	0	0	0	0	0	0	0	0	1^{Δ}
70 a An	2	Select cup 2	0	1^{Δ}	0	0	0	0	0	0	0	0	0	0	1^{Δ}
70 a An	3	Select cup 3	1^{Δ}	0^{Δ}	0	0	0	0	0	0	0	0	0	0	1^{Δ}
70 a An	4	Select cup 4	1^{Δ}	1^{Δ}	0	0	0	0	0	0	0	0	0	0	1^{Δ}
70 a An	1	Select cup 1	0^{Δ}	0^{Δ}	0	0	0	0	0	0	0	0	0	0	1^{Δ}
71 a 5P	1	Boom −0 volts (DC)	0	0	1^{Δ}	0	0	0	0	0	0	0	0	0	0
61 b 5B	1	Electron measurement Boom +25 volts (DC)	0	0	0^{Δ}	1^{Δ}	0	0	0	0	0	0	0	0	0
71 b 5M	1	Sets Monitor Mode Proton measurement Boom −25 volts (DC)	0	0	0	0^{Δ}	0	0	0	0	1^{Δ}	0	0	0	0
50 b 5S	1	Monitor measurement	0	0	0	0	0	0	0	0	1	0	0	0	0
50 a 5C	1	Step calibrate Selector Measurement Link check	0	0	0	0	0	0	0	1	0^{Δ}	0	0	1^{Δ}	0
50 a 5C	1	Temperature Measurement	0	0	0	0	0	0	0	1	0	0	1^{Δ}	1^{Δ}	0
50 a 5C	1	Frequency Measurement	0	0	0	0	0	0	0	1	0	1^{Δ}	0^{Δ}	1^{Δ}	0
50 a 5C	1	High-voltage Measurement	0	0	0	0	0	0	0	1	0	1	1^{Δ}	1^{Δ}	0
61 a 5A	1	Data Mode	0	0	0	0	0	0	0	0^{Δ}	0	0^{Δ}	0^{Δ}	0	0

line 45 receives two pulses and, since the multivibrator (MV) was turned "on" for a one-second interval by the previous command pulse, one of the gates at the input of the ES_0 flip-flop allows the first of the two command pulses to set ES_0 to the "one" state. Since the time between command pulses is 660 msec, the multivibrator that was turned "on" by the third command pulse, turns "off" before the second pulse occurring during the fourth command operation, and ES_0 is unaffected by this second pulse. Subsequent command functions are processed in a similar manner, and step the experiment through its operation.

Command lines 60 and a and b control the energy steps while command lines 70 and a control the selection of the cups. Command line 71 and line a control the boom potential, and command lines 61 and b determine whether the experiment measures protons or electrons. Command lines 71 and b control the Monitor Mode while lines 50 and b control the measurements during this mode. Raise trigger level (RTL) and lower trigger level (LTL) are used during the Monitor Mode to control the up-down counters.

4. Logic Circuit Functions

The eleven command lines containing Data Automation System signals are connected to the command conversion circuits where the command information is converted to digital signals which control the plasma probe experiment. The command conversion circuit contains nine heavy-duty logic buffers and the distribution circuit "and" and "or" gates. Figure 25 shows the logic circuits and Sec. III-D-5 describes individual logic-circuit elements.

a. Boom-Potential Input

The boom-potential input logic circuit and the flip-flop BP_1 convert the digital signals from the command conversion circuits to control the operation of relays R1, R4, and R6. These relays and their energizing driver amplifiers select the plasma probe boom-to-spacecraft-body potential required during the various plasma measurements.

b. Calibration Input

The calibration input logic circuit, with flip-flops CA_0 and CA_1, converts the digital signals from the command conversion circuits to control calibration points CA_1, CA_2, CA_3, and CA_4 during the calibration phase of the Data Mode.

c. Mode Input

The mode-input logic circuit, with flip-flops MD_0 and MD_1, controls proton and electron phases of the Data Mode measurements. This circuit also controls the Monitor Mode.

d. Proton-Electron Input

The proton-electron logic circuit, with flip-flop PE, operates relay R3 through a relay driver. This circuit determines the plasma measurement (proton or electron) to be made.

e. Cup Gate Input

The cup gate logic circuit, flip-flops CS_0 and CS_1, and the associated output logic circuit, select the cup gate to be activated. Monostable multivibrator DS controls the plasma measurement phases so that cup gates 1, 2, 3, and 4 are activated sequentially during the Data Mode and simultaneously during the Monitor Mode.

f. High-Voltage Level Input

The high-voltage logic circuit, flip-flops ES_0, ES_1, and ES_2 and the associated output logic circuit determine the operation of the digital high-voltage level control circuits. The monostable multivibrator (MV) controls the sequence. In the Data Mode the eight incremental high-voltage levels applied to the faraday cup grids are controlled by activating the logic circuit sequentially (for levels one to eight). In the Monitor Mode the eighth level is selected unless otherwise directed by the ground station.

g. Monitor Input

The monitor logic circuit, with flip-flops FF_1, FF_2, and FF_3, operates the up-down counter (in the monitor circuit) on command from the ground station through lines RTL (raise trigger level) and LTL (lower trigger level). When power is first applied to the plasma probe the up-down counter is preset to a high level (6 volts). This level is reduced by a -3-volt potential from the LTL line. To change the up-down counter from low to high level requires a -3-volt pulse on the RTL line. The counter will then return to the 6-volt level.

5. Logic Circuit Description

The following circuit descriptions explain the basic design requirements and describe the operation of each logic circuit.

a. Heavy Duty Logic Buffer

The logic circuit contains nine identical heavy duty (2-transistor) logic buffers. Figure 27 is a schematic diagram of a logic buffer. The logic buffer design was based on the following requirements:

Present a 5-kohm load to the Data Automation System

Minimize digital noise

Shape and isolate the input 40-μsec pulse from the Data Automation System circuits.

Because of the differences in potential between the spacecraft and the plasma probe experiment, each logic buffer is capacitively coupled to the main spacecraft.

To reduce digital noise the input diode is forward-biased, which back-biases the first transistor (Q34) of the buffer by -0.7 volt. The first stage of the buffer is biased "off" and the second stage remains "on." This terminology assumes that: (a) an "on" stage is represented by a voltage near ground, and (b) an "off" stage is represented by a voltage approaching the given supply voltage.

When a +6-volt signal is applied to the buffer from the Data Automation System, the first stage (Q34) goes "on" and the second stage (Q35) goes "off" for the duration of the pulse. Assuming a beta of 20, the buffer is capable of driving a 310-ohm load. The 4-volt signal developed by the buffer is applied to the input logic circuits.

b. Input Logic Circuits for Flip-Flop

The plasma probe program logic utilizes -3-volt trailing-edge logic to set or reset the binary flip-flops. The 4-volt pulse from the logic buffer drives either an "and" or an "or" gate.

The "and" gate, shown in Fig. 28, has from two to four inputs. Under normal conditions the "and" gate is at ground potential. When all inputs to the gate receive a positive, 40-μsec, 3-volt signal, the gate is charged to 3 volts through the "and" gate diode-bias resistor. Upon completion of the gate pulse the negative portion of the differentiated pulse is applied to the base of the "on" transistor of the binary flip-flop, causing the "on" transistor to be turned "off." The positive portion of the differentiated pulse is clipped by the forward-biased digital noise diode. The "or" gate is similar to the "and" gate except for the single input at the base of the binary flip-flop.

c. Binary Transistor Flip-Flops

Eleven identical transistor flip-flops are used as the binary elements in the plasma probe unit. The flip-flop circuit is shown schematically in Fig. 29. It is essentially a standard Eccles-Jordan circuit (saturated design). The design of this flip-flop is based on the following requirements:

High stability and reliability

Low power drain

Minimum number of transistors (per binary) and ability to drive a 2.5-kohm load.

The circuit is designed to drive a 2.5-kohm load and has a DC beta of 20. The transistors used have a beta of 40 (at room temperature) which provides a considerable margin for circuit operation and aging. Each flip-flop is designed to draw approximately 5.5 mw from the supply.

d. Basic Monostable Multivibrator

Two identical transistor monostable multivibrators are used as binary reset elements in the plasma probe. The design of the monostable multivibrator is based on the following requirements:

Long time-period

Low power drain

Capability of driving a 3-kohm load.

The standard transistor monostable multivibrator used (see Fig. 30) has been modified so that the input circuit is a ground-base stage which is biased "off" by +0.7 volt to minimize digital noise.

When a −3-volt signal is applied to the emitter of the grounded-base stage, the transistor is turned "on" and the negative signal from the collector of Q35 turns "off" the normally "on" transistors Q36 and Q37. To prevent base-to-emitter breakdown when the capacitor voltage is negative, a diode is placed in series with the base of Q36. When the transistors Q36 and Q37 are turned "off," the normally "off" transistors Q38 and Q39 are turned "on" for a duration determined by the RC time constant of the monostable multivibrator.

The monostable multivibrator will operate over an ambient temperature range of −50° to +125°C and requires approximately 7 milliwatts of operating power.

e. Relay Drivers

The plasma probe uses four relays to switch potentials related to logic circuit operation.

The driving circuit for the miniature magnetic-latching DPDT relays is shown in Fig. 31. When the signal on the base of Q40 is at ground potential the collector is at the supply voltage potential. The collector of Q40 drives a complementary emitter-follower. With the collector of Q41 positive, the capacitor in series with the relay field coil is charged. A voltage of +3 at the base of Q40 will cause the collector to approach ground potential and turn "on" Q42, discharging the capacitor in series with the field coil of the latching relay. The relay will not respond to a step function; therefore, a simple series RC network is placed in series with the relay coil to produce a 20-msec pulse. Relay latching is determined by the current flow through the coil.

IV. PLASMA PROBE EXPERIMENT – TEST AND CHECKOUT

A. General

This section describes the various tests required to determine the operational status of the plasma probe equipment. All significant waveshapes and voltages associated with each section are discussed.

B. Measurement Link

A block diagram showing test points, required test equipment, and connections to the measurement link for checkout is given in Fig. 32. In addition to the test equipment shown, an oscilloscope (Tektronix No. 545 or equivalent) with a 53/54L preamplifier is required to monitor the test points.

1. Preamplifier

A 2-kcps signal (0 to 6 volts) is applied to the microvolter from the modulator flip-flop in the high-voltage section. (The modulator generator 4-kcps signal must be within ±5 cps maximum at room temperature.) Microvolter output at 1 volt peak-to-peak (2 kcps) is applied to test point P. A. at one of the four preamplifiers.

This 1-volt signal at test point P. A. simulates the maximum plasma current level of 10^{-7} amp from the faraday cup. The multiplier on the microvolter is used to reduce the 1-volt input at test point P. A. by decades. The lowest plasma-current level detected by the faraday cup is 10^{-12} amp, which can be simulated by reducing the 1-volt signal from the microvolter five decades with the multiplier control. Intermediate steps are obtained by setting the microvolter to the required level. This method is used to obtain a telemetry curve described later in this section.

With 1-volt peak-to-peak applied at test point P. A., the output of the preamplifier at test point P. A. O. will be approximately 0.9 to 1.0 volt (peak-to-peak) into a 24-kohm load (or into the following cup gate). Signal output data at test point P. A. O. is given in Table IV, item 2. The broad-band noise at test point P. A. O. measured with the Tektronix 545 oscilloscope and 53/54L preamplifier head should not be greater than 3 mv peak-to-peak. The narrow-band noise (500 cps) should be approximately 25 microvolts.

2. Cup Gate

Each preamplifier is followed by a cup gate which is controlled by a 3-volt logic level pulse. When a 3-volt level is applied to either CG1, CG2, CG3 or CG4, the gate is "on" and is capable of passing a signal from its preamplifier to the summation amplifier. Connect the microvolter

to test point P. A. of each preamplifier successively, and check the output of each associated cup gate separately. The voltage gain before the 20-kohm adder resistor of each cup gate is approximately 1.7.

3. Summation Amplifier

The summation amplifier amplifies the signal from the gate circuit resistive adder network and provides a low-impedance drive to the active twin-T filter. The over-all gain of the cup gate and summation amplifier is roughly 2. For signal characteristic data at test point F1, see Table IV, item 3. Apply a test signal from the microvolter as described in Sec. IV-B-1.

4. Active Twin-T Filter

The active twin-T filter circuit is basically an amplifier with a twin-T filter in its negative feedback loop. The amount of feedback at the null frequency is approximately zero, and the gain of the amplifier at the null frequency is the same as the gain of the amplifier without feedback. On either side of the null frequency the feedback increases and the amplifier gain will be reduced proportionally.

The gain of the amplifier at the null frequency is 2 and the bandwidth is ±200 cps at 2 kcps. The output of the amplifier will contain the 2-kcps fundamental with some 2nd harmonic. For signal characteristics data at test point F2 see Table IV, item 4. Apply a test signal from the microvolter as described in Sec. IV-B-1.

5. Compression Amplifier

To cover a 5-decade range, the gain of each stage in the compression amplifier is approximately 3.2. The last amplifier stage saturates first and the first stage last. The outputs of every other stage are summed and combined at a summing point. For signal characteristic data at the output of the compression amplifier refer to test point C2 and Table IV, item 5. Apply a test signal from the microvolter as described in Sec. IV-B-1.

6. Synchronous Detector

The synchronous detector performs two operations. The first operation sums the outputs of the compression amplifier by means of a common-base transistor stage driving a balanced transformer. The output of this transformer drives an emitter-follower which drives the synchronous detector. Gain adjustment of the synchronous detector output is controlled by the 10-kohm potentiometer. For signal characteristics data at test point C2 refer to Table IV, item 5. Apply a test signal from the microvolter as described in Sec. IV-B-1.

The second function of the synchronous detector is to convert the output of the compression amplifier to a DC analog signal. The 2-kcps (modulated) signal from the compression amplifier is mixed with a 2-kcps carrier producing an analog output ranging from 0.5 to 5.5 volts. A typical analog output at test point 2 with test point 1 grounded is given as item 6 in Table IV.

C. High-Voltage Supply

The checkout procedures for the high-voltage supply are divided into two groups. Group 1 procedure checks the regulator circuit in the digital high-voltage level control which establishes the primary voltage for the step-up high-voltage transformer. Group 2 procedure checks the high-voltage increments working into a 240-pf load. The high-voltage supply is disconnected for the tests of Group 1.

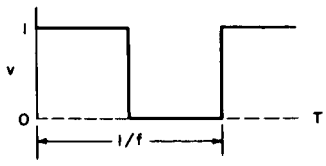
TABLE IV

MEASUREMENT LINK SIGNAL DATA*

1. Test Signal, Test Point P.A.

		Impedance (Ω) In	Impedance (Ω) Out
From:	Microvolter	600	600
To:	Preamplifier	500 k	200
Frequency:	2-kcps square wave		
Signal Range:	1 ± 0.1-v pp		

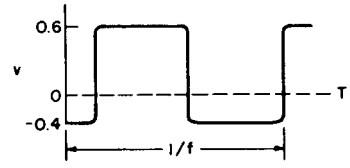
Signal Waveform



2. Preamplifier Output, Test Point P.A.O.

		Impedance (Ω) In	Impedance (Ω) Out
From:	Preamplifier	500 k	200
To:	Cup gate	24 k	20 k
Frequency:	2-kcps square wave		
Signal Range:	1 ± 0.1-v pp		
Noise:	BB ⩽ 3.5-mv pp NB ⩽ 25 μv (500 cps) at 2 kcps		

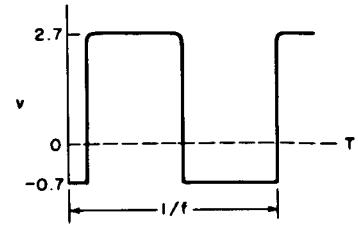
Signal Waveform



3. Cup Gate and Summation Amplifier, Test Point F1

		Impedance (Ω) In	Impedance (Ω) Out
From:	Summation amplifier output	20 k	100
To:	Twin-T input	9 k	200
Frequency:	2-kcps square wave		
Signal Range:	2 ± 0.2-v pp		

Signal Waveform



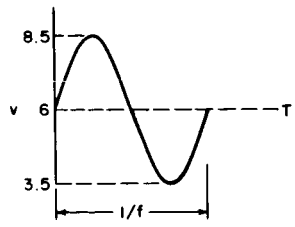
*See Fig. 32.

TABLE IV (Continued)

4. Active Twin-T Filter Output, Test Point F2

		Impedance (Ω) In	Impedance (Ω) Out
From:	Twin-T filter	10 k	4 k
To:	Compression amplifier	5 k	10 k
Frequency:	2-kcps sine wave		
Signal Range:	5 ± 0.2-v pp		
Filter Bandwidth:	±200 cps		

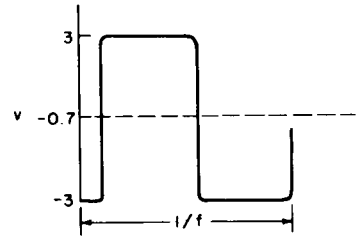
Signal Waveform



5. Compression Amplifier, Test Point C2

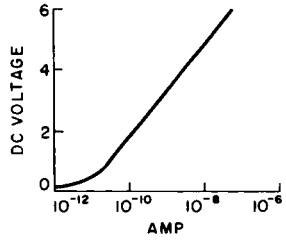
From:	Compression amplifier
To:	Synchronous detector
Frequency:	2 kcps
Signal Range:	6 ± 0.3-v pp

Signal Waveform



6. Analog Output, Test Point 2

From:	Synchronous detector
To:	DAS
Signal Range:	0.5 to 5.5 v ± 3 % linear



1. Group 1

Group 1 provides a 3-kohm load for the regulator circuit. The voltage across the load for each step should be as follows:

Step	Voltage	ES_2	ES_1	ES_0
1	−0.25	0	0	0
2	−0.50	0	0	1
3	−0.94	0	1	0
4	−1.80	0	1	1
5	−3.7	1	0	0
6	−7.1	1	0	1
7	−14.5	1	1	0
8	−27.5	1	1	1

2. Group 2

Group 2 procedures are divided into two sections.

a. Section 1

This section consists of measurements of high-voltage increments while the plasma probe is in the proton measurement phase. The voltage increments at the load (240 pf) for each step are as follows:

Voltage Step	Voltage	Tolerance (volts)	ES_2	ES_1	ES_0
1	−2.5 to +7.5	±0.5	0	0	0
2	+5 to +15	±1	0	0	1
3	+10 to +58	±1	0	1	0
4	+40 to +120	±4	0	1	1
5	+100 to + 300	±10	1	0	0
6	+200 to +600	±20	1	0	1
7	+500 to +1500	±50	1	1	0
8	+1000 to +2800	±150	1	1	1

b. Section 2

With the plasma probe in the electron measurement phase of the Data Mode, the high-voltage increments are as follows:

Voltage Step	Voltage	Tolerance (volts)	ES_2	ES_1	ES_0
1	+2.5 to −7.5	±0.5	0	0	0
2	−5 to −15	±1	0	0	1
3	−10 to −58	±1	0	1	0
4	−40 to −120	±4	0	1	1
5	−100 to −300	±10	1	0	0
6	−200 to −600	±20	1	0	1
7	−500 to −1500	±50	1	1	0
8	−1000 to −2800	±150	1	1	1

D. Ancillary Circuits

Block diagrams which show the test setup for checking the calibrate and monitor circuits are given in Figs. 32 and 33.

1. Calibrate Circuit

The first of four pulses on line 50a of the Data Automation System simulator causes a 2-kcps internal test signal to be sent through the measurement link. The pulse sets up a 3-volt level at point CA1 in the calibrate logic circuits, which inserts the test signal at the summation amplifier. Normal operation is indicated by a reading of +3.0 ± 0.5 volts DC at Analog Output (test point 2) with test point 1 grounded.

The second pulse on line 50a initiates a temperature measurement by the calibrate circuits. The pulse sets up a 3-volt level at point CA2 in the calibrate logic circuits. The analog output which corresponds to 20°C is 3.0 ± 0.5 volts DC at test point 2 with test point 1 grounded.

The third pulse on line 50a initiates a frequency check by the calibrate circuits. A 3-volt level is established at point CA3 in the calibrate logic circuits which causes the calibrate circuits to check the system clock frequency. Normal frequency operation is indicated by an analog output level of +1.5 ± 0.5 volts DC at test point 2 with test point 1 grounded.

The fourth pulse on line 50a causes the calibrate circuits to measure the operation of the modulator driver circuits. The pulse sets up a +3-volt level at point CA4 in the calibrate logic circuits which initiates a measurement of the chopped voltage at the modulator driver. Normal circuit operation is indicated by an analog output level of +0.25 volt DC at test point 2 with test point 1 grounded.

2. Monitor Circuits

The monitor circuits are included in the plasma probe instrumentation to increase the measurement flexibility of the system (see Sec. II-C-5b). It was desirable to include an "automatic" monitoring feature which would automatically place the system in the measurement mode when plasma intensity exceeded a preset level (adjustable in flight command). This was accomplished by including circuits in the system which compare the voltage signals from the measurement link with an adjustable reference voltage level. When the plasma intensity exceeds this reference level a signal is sent to the Data Automation System which switches the experiment into the Data (measurement) Mode. The adjustable level requirement is obtained from a resistor ladder network connected to an "up-down" binary counter as shown in Fig. 34.

The equations shown in Fig. 34 give the expressions governing the clocking conditions of a binary scaler operated as a reversible add or subtract scaler. (A count of one is obtained from the scaler for each pulse received.) The output from the resistor network is a voltage between zero and six volts and is a function of the binary number contained in the scaler.

3. Logic Circuits

A block diagram of the test setup and connections for checking the logic circuits is given in Fig. 35. The test equipment required to perform the checkout procedure includes a Data Automation System simulator and a light indicator.

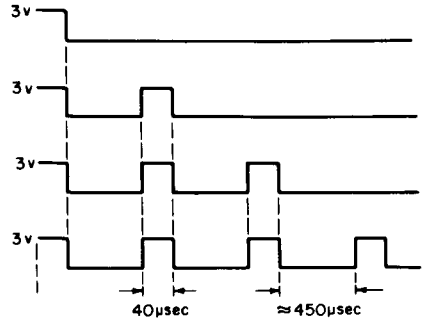
The Data Automation System simulator will supply all commands and any sequence of command pulses for test purposes. For example, if a single 40-μsec pulse is required for line 61

TABLE V

LOGIC SECTION SIGNAL DATA*

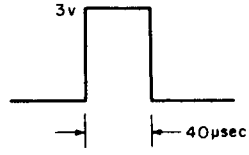
1. DAS Output (A)

From:	Data automation system
To:	Heavy duty logic buffer
Signal Range:	3 v
Rise Time:	⩽15 μsec
Fall Time:	⩽15 μsec
Pulse Width:	≈40 μsec



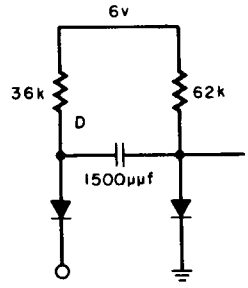
2. HLB Output (B and C)

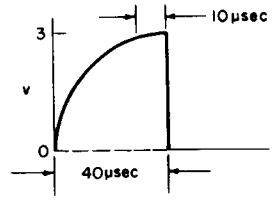
From:	Heavy duty logic buffer
To:	Gate
Signal Range:	3 v



3. RCD Input (D)

From:	Gate
To:	Flip-flop
Signal Range:	3 v



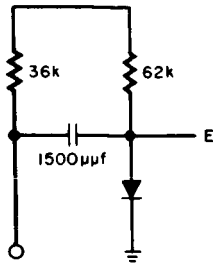


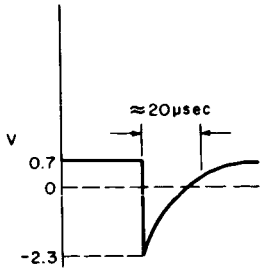
*See Fig. 32.

TABLE V (Continued)

4. RCD Output (E)

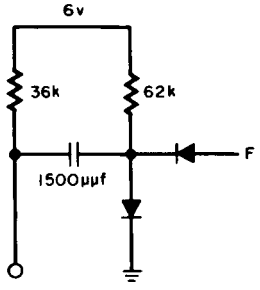
From: Gate
To: Flip-flop
Signal Range: 3 v

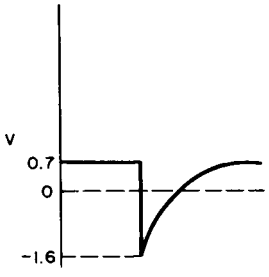




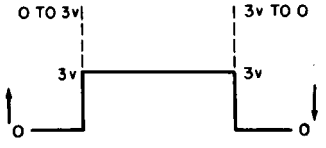
5. RCD Output (F)

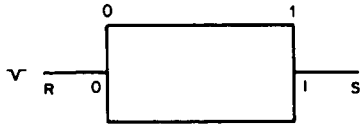
From: RCD
To: Flip-flop





6. Basic Flip-Flop





and line a, the operator depresses the "one-pulse" button (on the Data Automation System simulator), throws the line 61a toggle switch, and then presses the START button. This action sends a 3-volt, 40-μsec pulse down lines 61 and a. To obtain other pulses for a given line a different pulse selector button is used.

The plasma probe under test has 11 marked test points to indicate the "one" side of the 11 flip-flops to be checked. The light-indicator lines are connected directly at these 11 flip-flop test points. The light indicator shows the state of a particular flip-flop after a given logic command.

The command sequences for checking the logic circuits, given in Tables III and IV, are as follows. With the plasma probe and test equipment connected as shown in Fig. 33, perform the operations listed in the command column. After each command, compare the light pattern on the light indicator with the Truth Table binary state column. In both tables the delta (Δ) represents a change of state.

When checking the plasma probe it must be kept insulated from ground, and the Data Automation System simulator common must be connected to Data Automation System simulator ground. This simulates conditions encountered in the spacecraft and duplicates the potential difference between the plasma probe and the spacecraft.

E. Logic Philosophy

The command conversion circuits utilize 3-volt, negative trailing-edge pulses. Refer to Fig. 33 and the Table V waveforms for a check of circuit operation.

In Table V, item 1, Data Automation System output is approximately 3 volts obtained from a 5-kohm source. Item 2 is the HLB output from the buffer and drives an RCD "and" gate. The anode side of the RCD is shown in item 3. Item 4 is the differentiated pulse from the RCD. The pulse which sets or resets the flip-flop is shown as item 5 in Table V. The logic levels, where a "zero" is a ground potential and a "one" is at a 3-volt potential, are shown in item 6.

F. Power Supply Requirements

A total of eight DC voltages are required to operate the plasma probe unit. These are derived from the spacecraft power by conventional unregulated power supplies using RC and LC filters. Voltages and currents are shown in Table VI. With the exception of the boom potentials, which are available on the GSE connector, no provision is made to monitor the power-supply voltages externally.

TABLE VI
POWER SUPPLY REQUIREMENTS

Voltage (DC)	Current (ma)	Voltage (DC)	Current (ma)
+20	12	−30	75
+6	84	+100	0.1
−6	44	+100	0.1
+12	56	+650	0.05

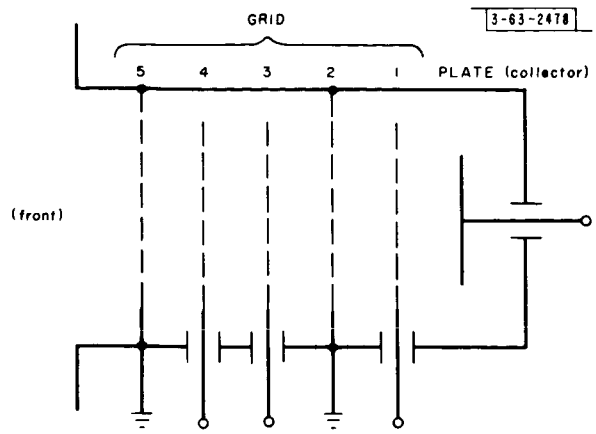


Fig. 1. Faraday cup.

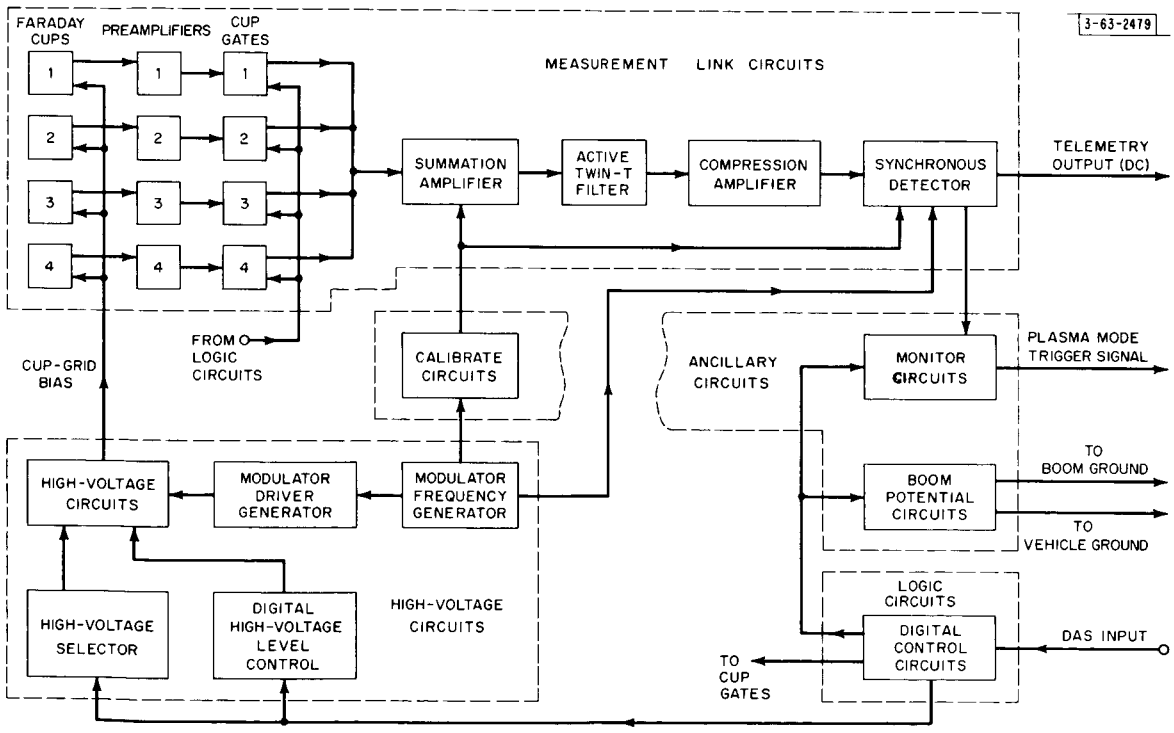


Fig. 2. Plasma probe instrumentation.

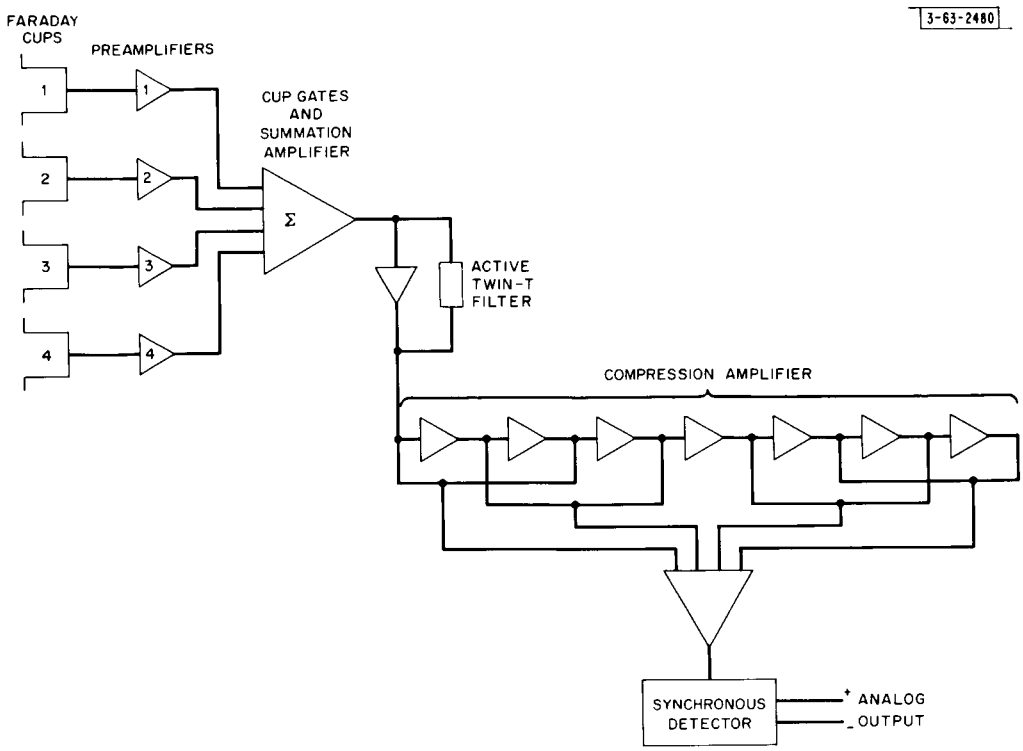


Fig. 3. Measurement link.

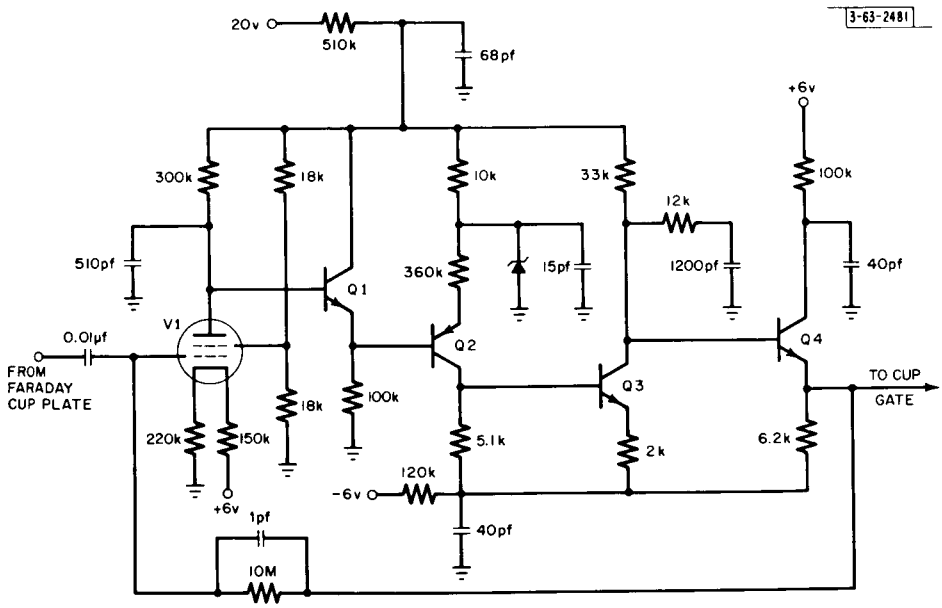


Fig. 4. Preamplifier, schematic diagram.

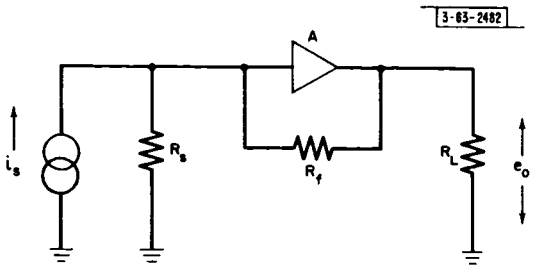
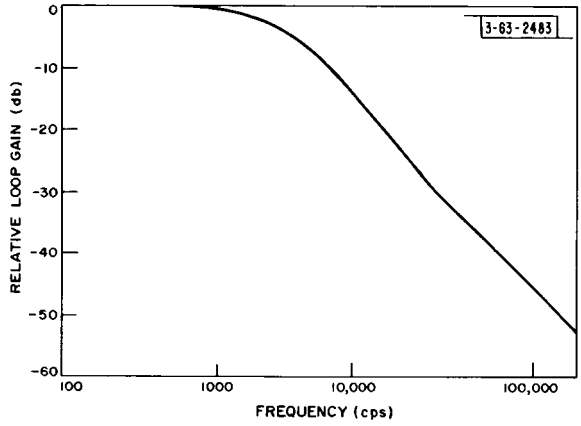


Fig. 5. Preamplifier, functional diagram.

Fig. 6. Preamplifier, loop gain vs frequency.



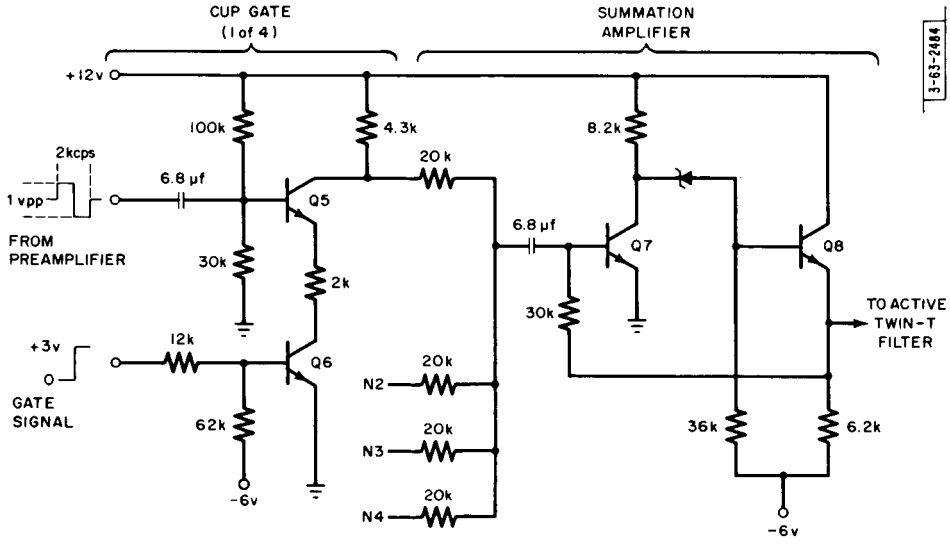


Fig. 7. Cup gates and summation amplifier.

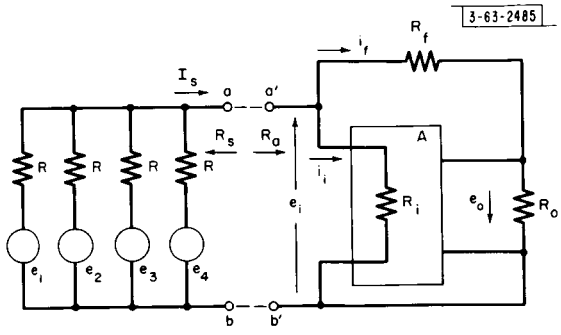


Fig. 8. Summation amplifier.

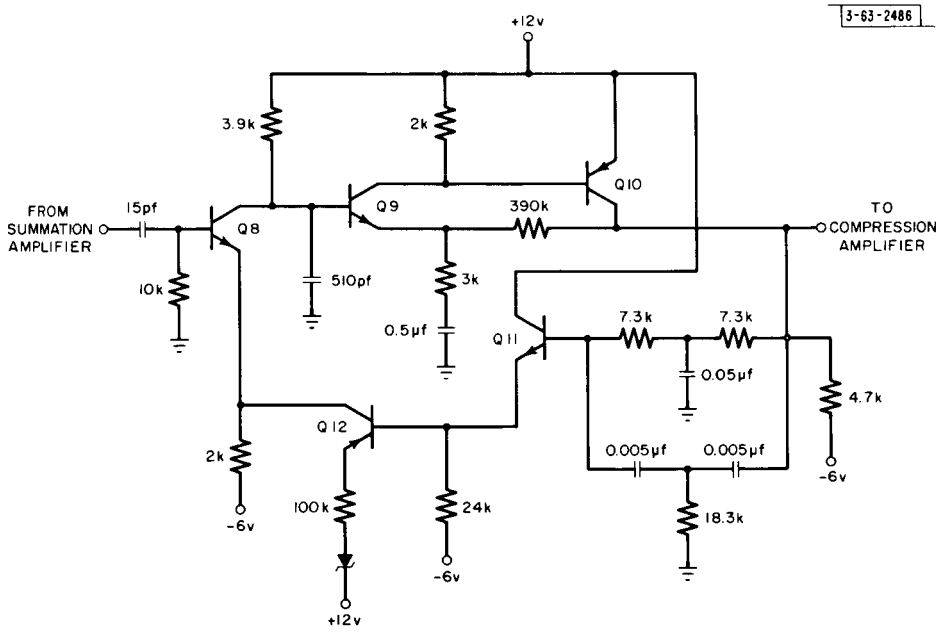


Fig. 9. Active twin-T filter, schematic diagram.

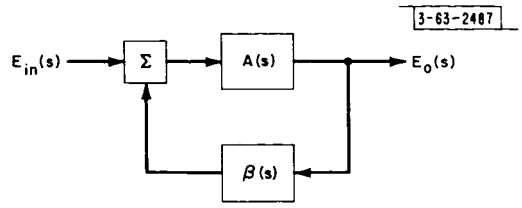


Fig. 10. Active twin-T filter, block diagram.

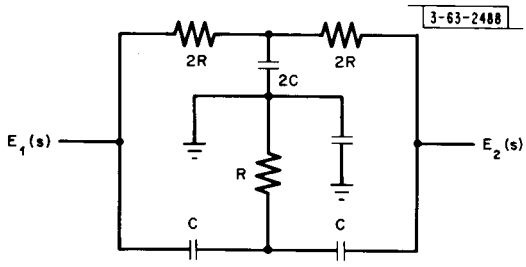


Fig. 11. Twin-T filter, network diagram.

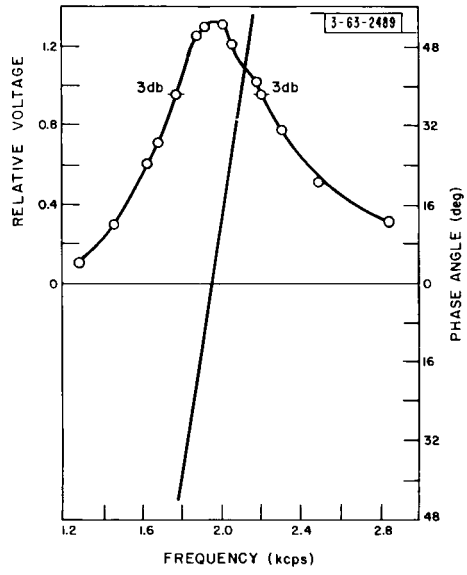


Fig. 12. Active twin-T filter, amplitude response curve.

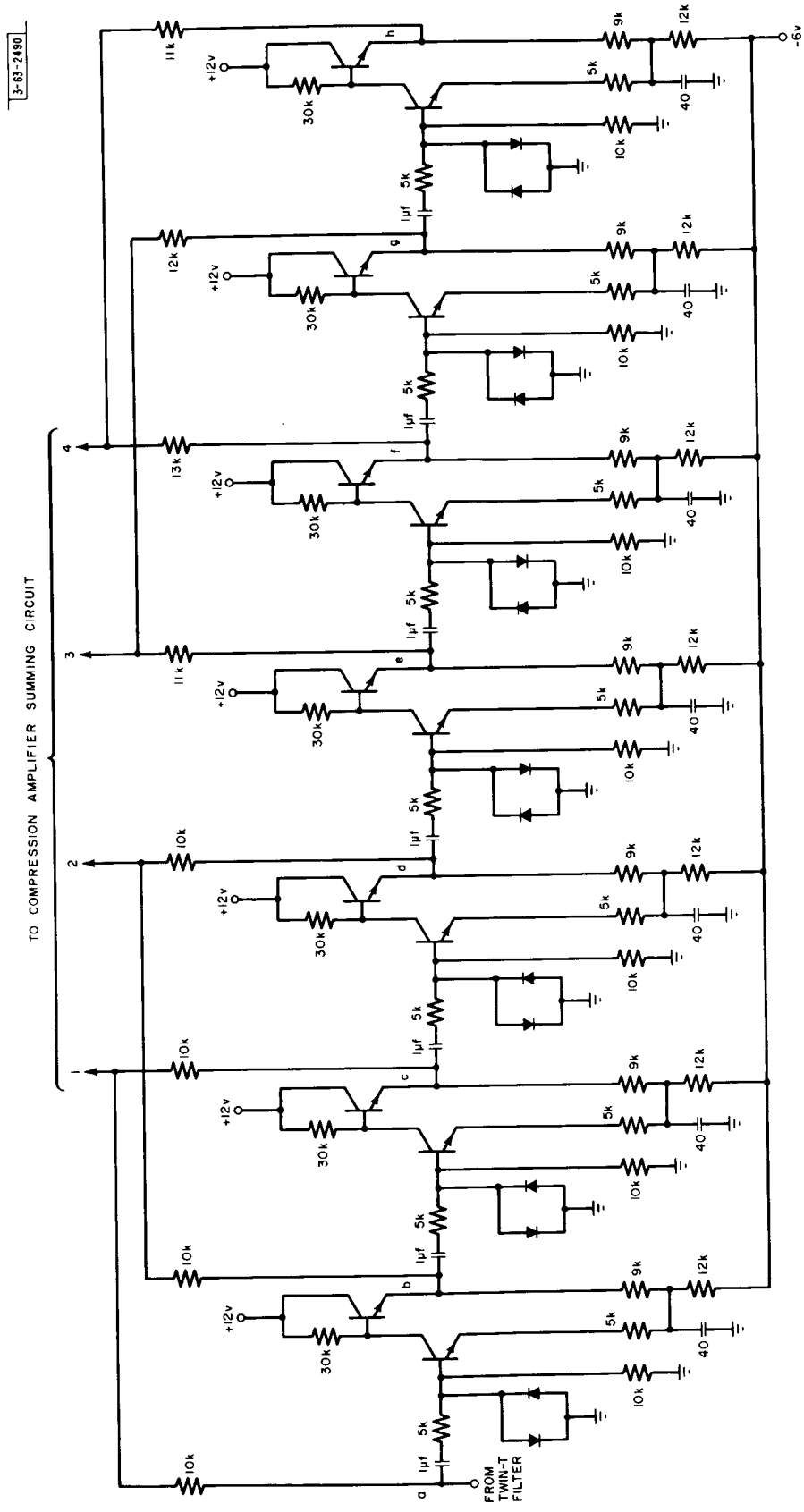


Fig. 13. Compression amplifier.

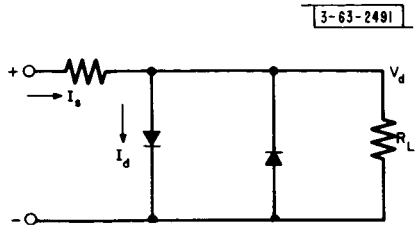


Fig. 14. Logarithmic limiting network.

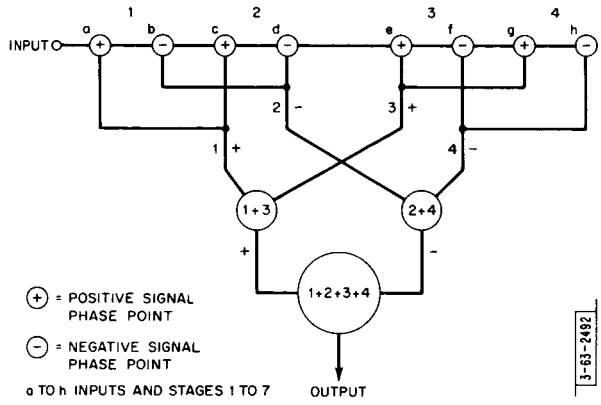


Fig. 15. Compression amplifier.

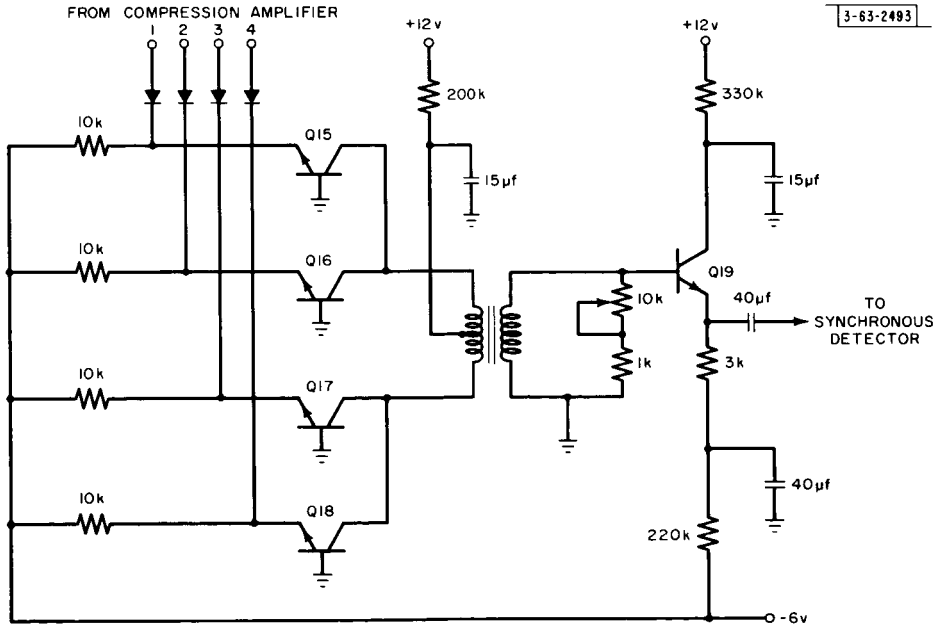


Fig. 16. Compression amplifier summing circuit.

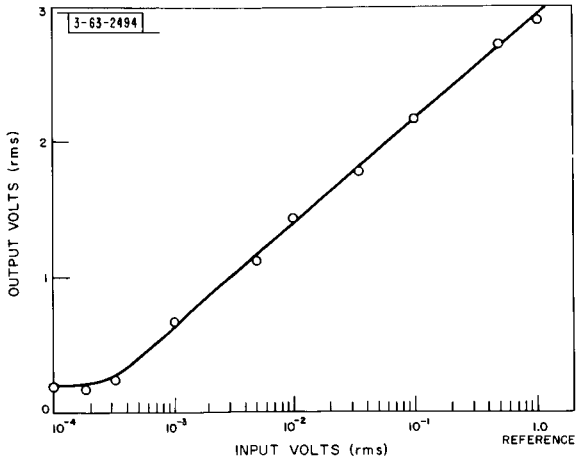


Fig. 17. Compression amplifier, output vs voltage.

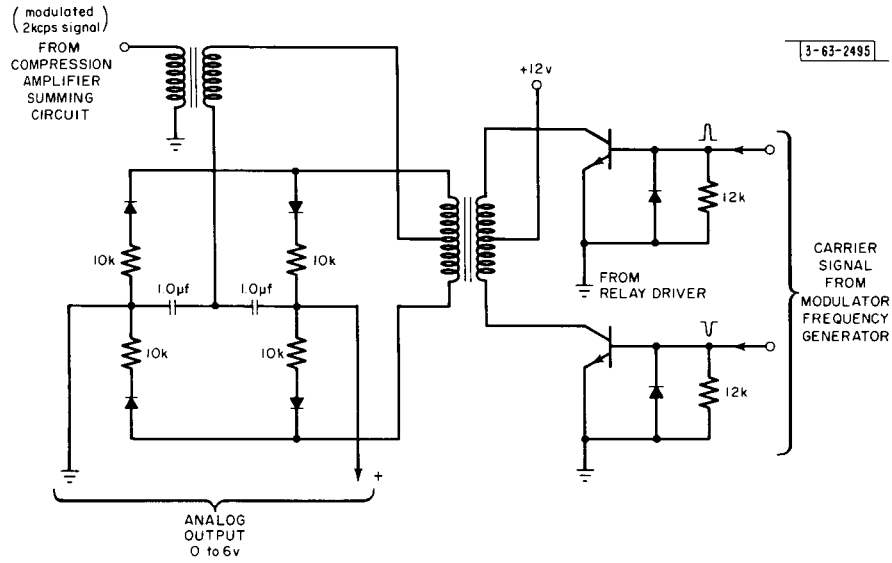


Fig. 18. Synchronous detector.

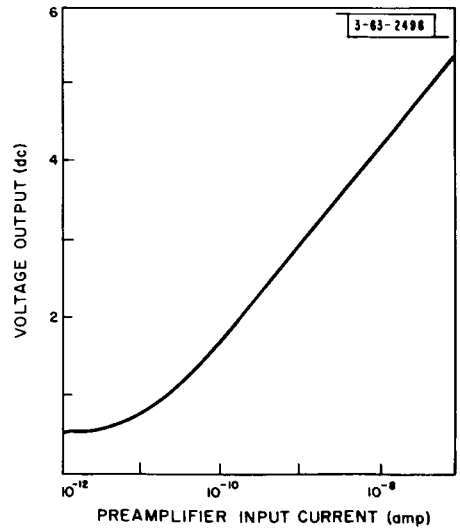


Fig. 19. Analog curve, preamplifier input vs synchronous detector output.

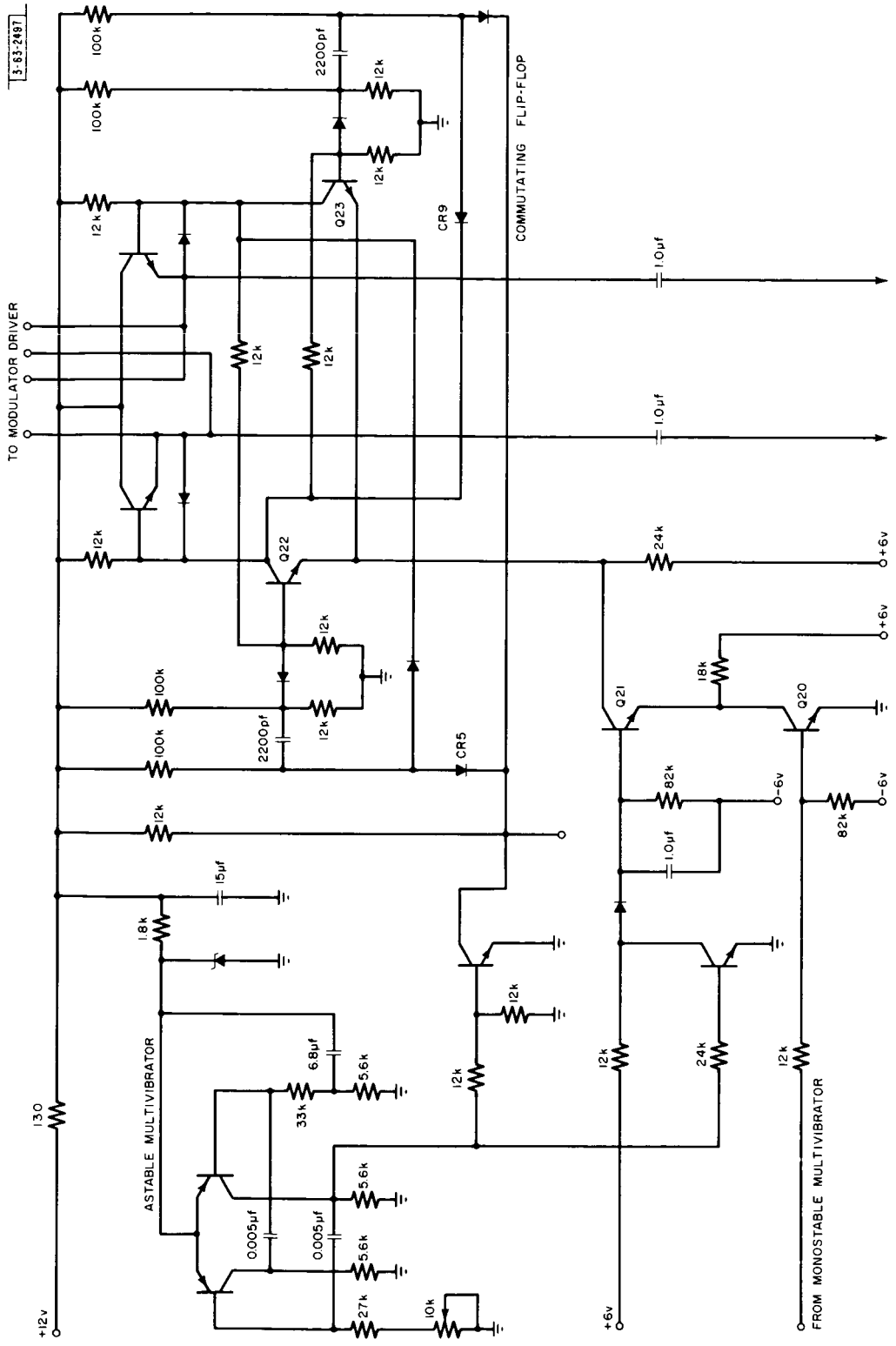
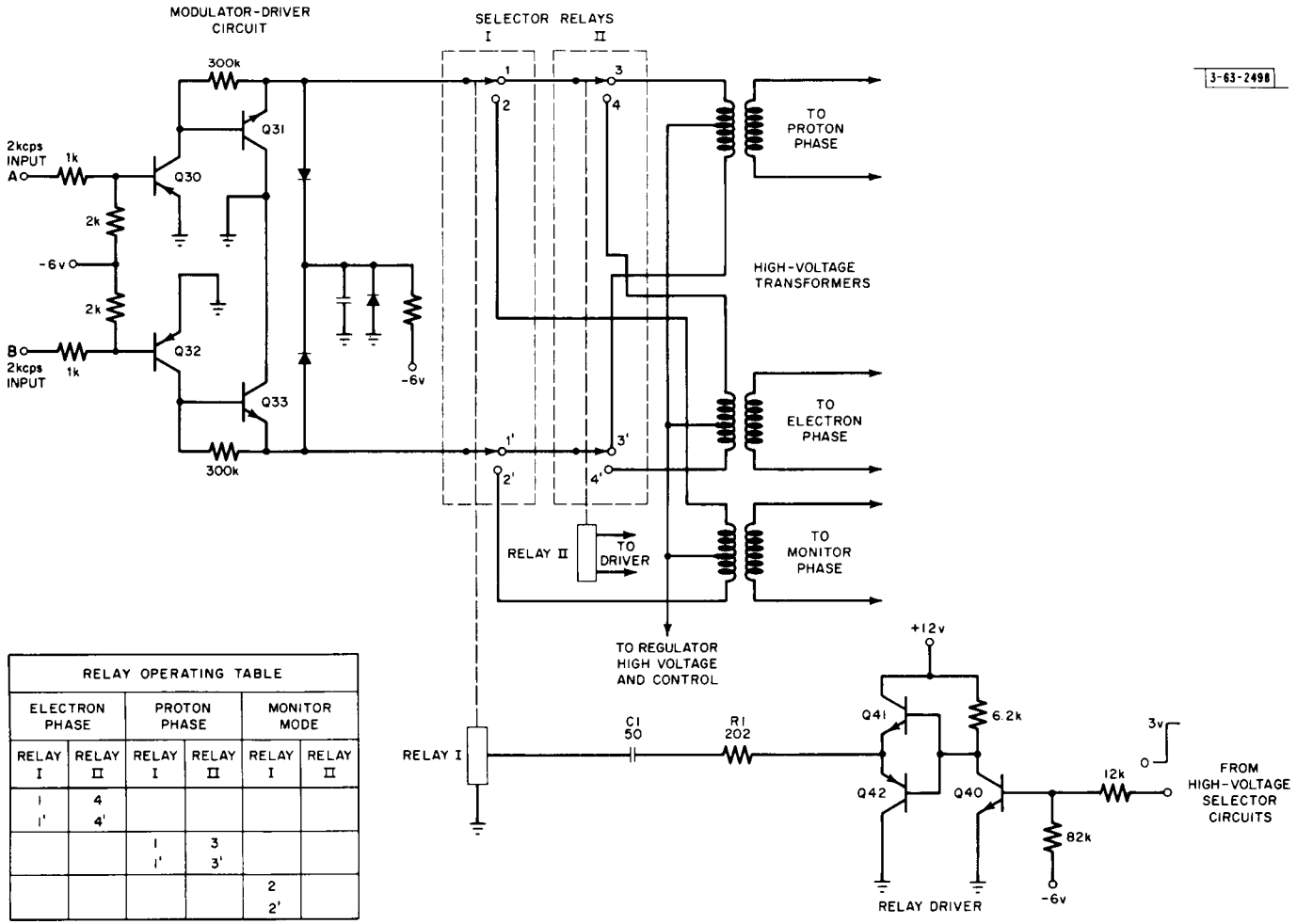


Fig. 20. Modulator frequency generator.



RELAY OPERATING TABLE					
ELECTRON PHASE		PROTON PHASE		MONITOR MODE	
RELAY I	RELAY II	RELAY I	RELAY II	RELAY I	RELAY II
1 1'	4 4'				
		1 1'	3 3'		
				2 2'	

Fig. 21. Modulator driver and high-voltage selector circuit.

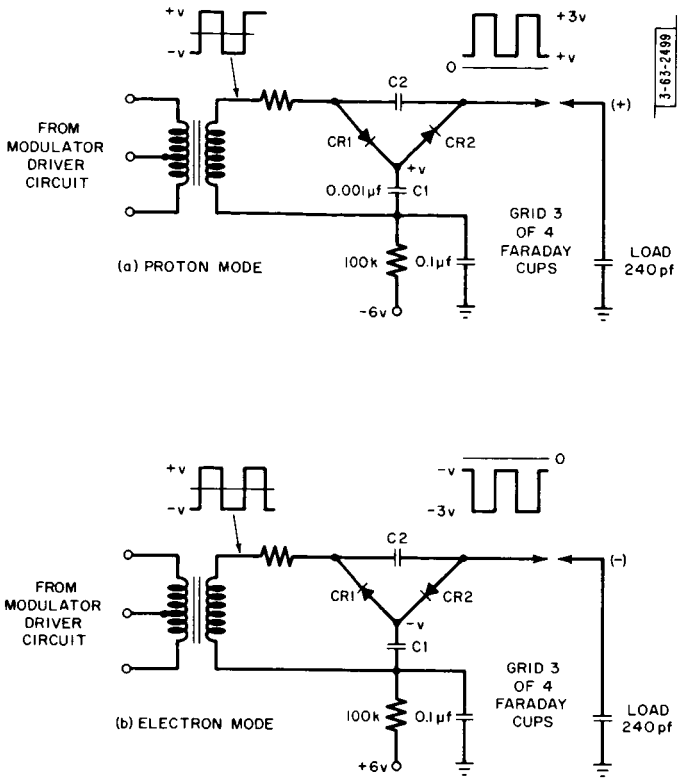


Fig. 22. Voltage doublers.

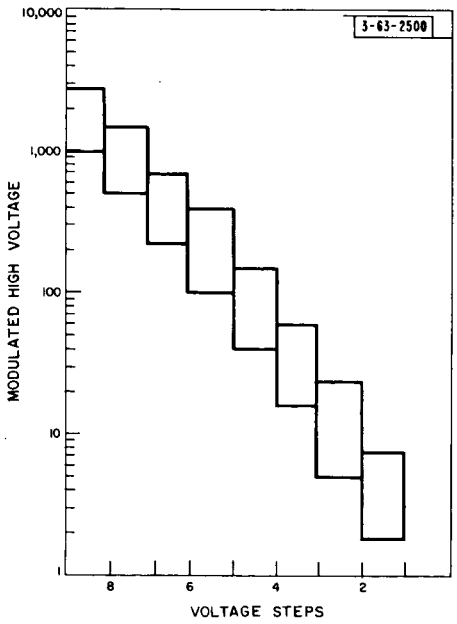


Fig. 23. High-voltage supply, incremental steps.

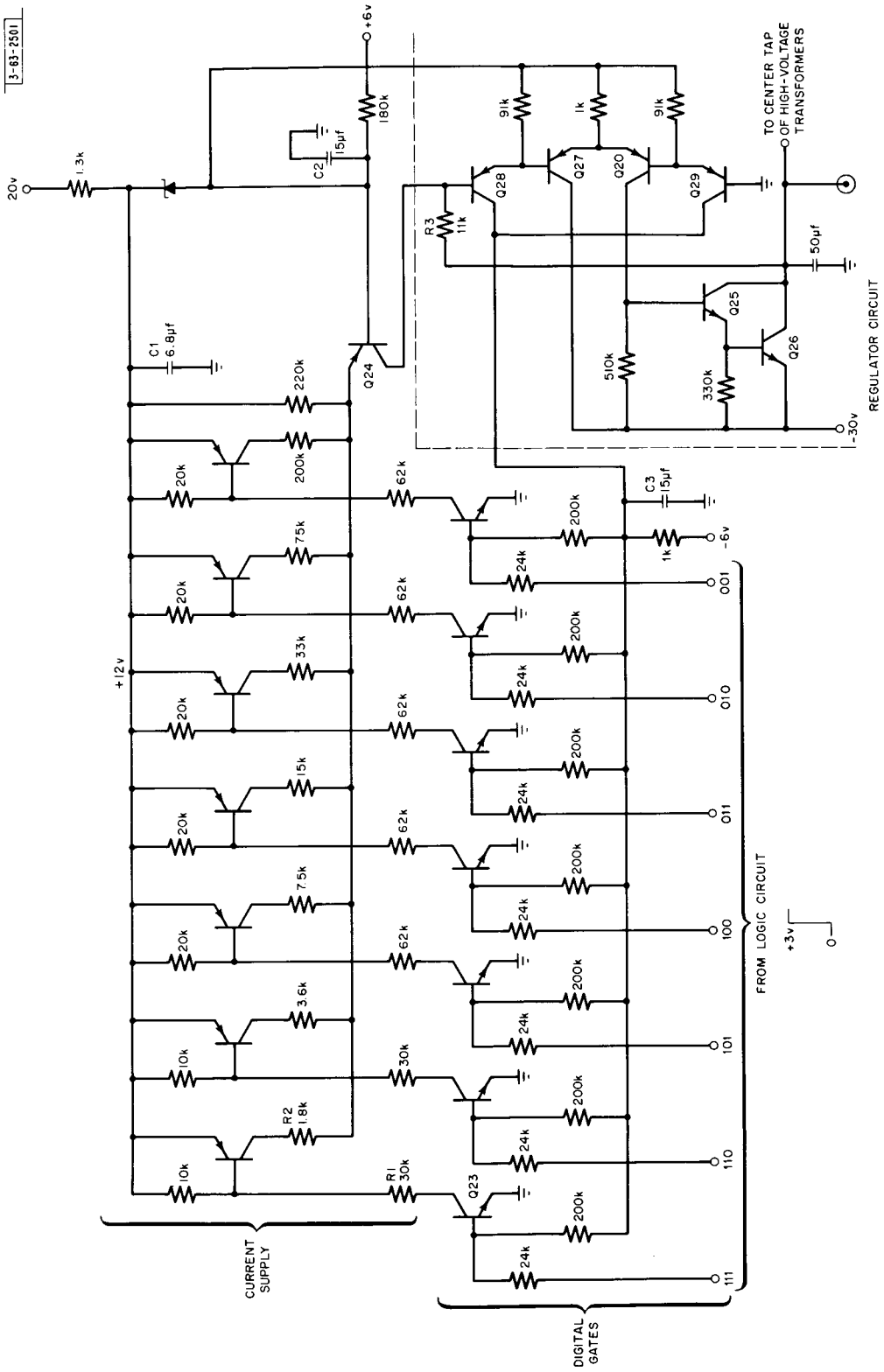


Fig. 24. Digital high-voltage control.

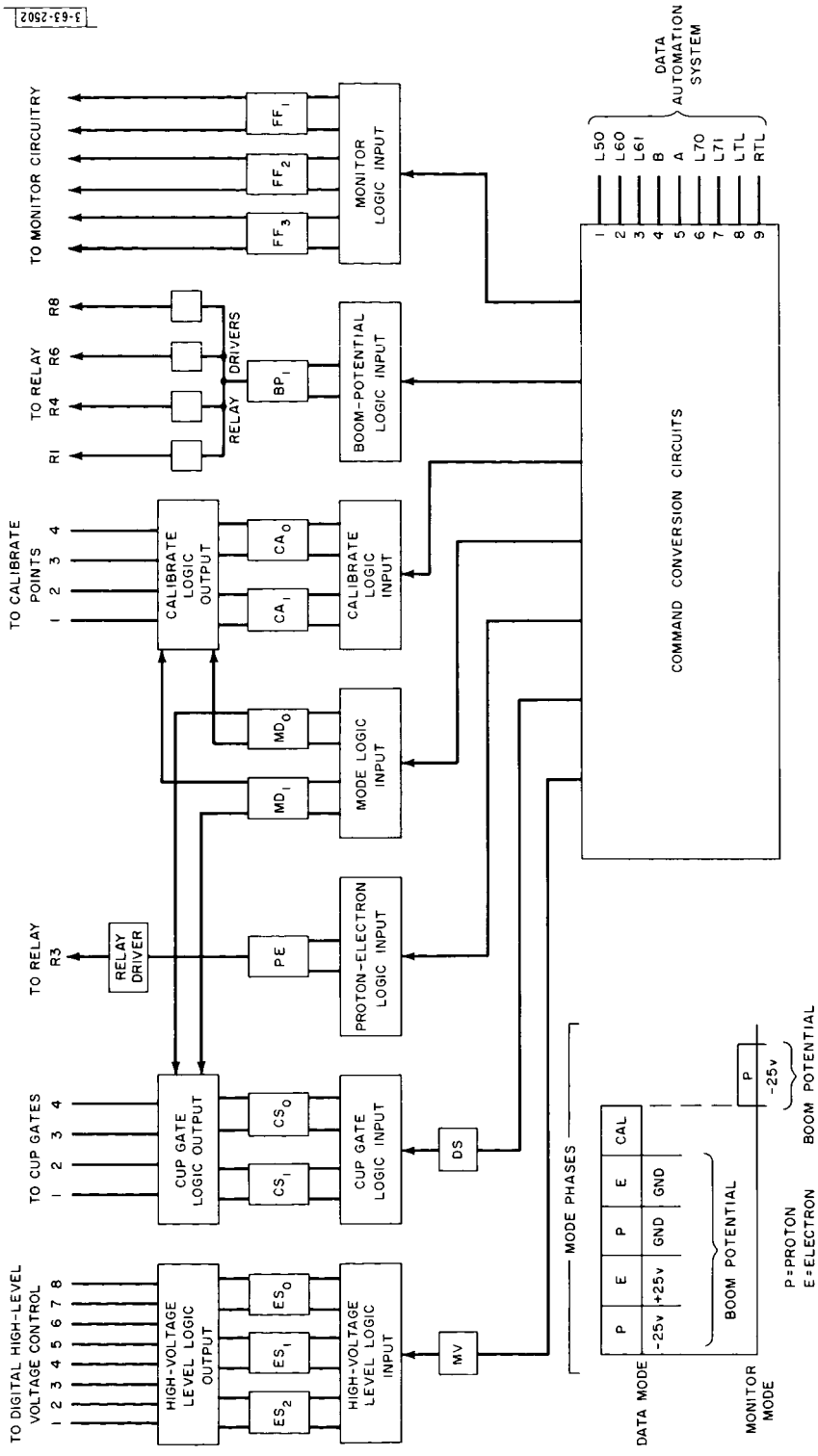


Fig. 25. Logic circuit, simplified block diagram.

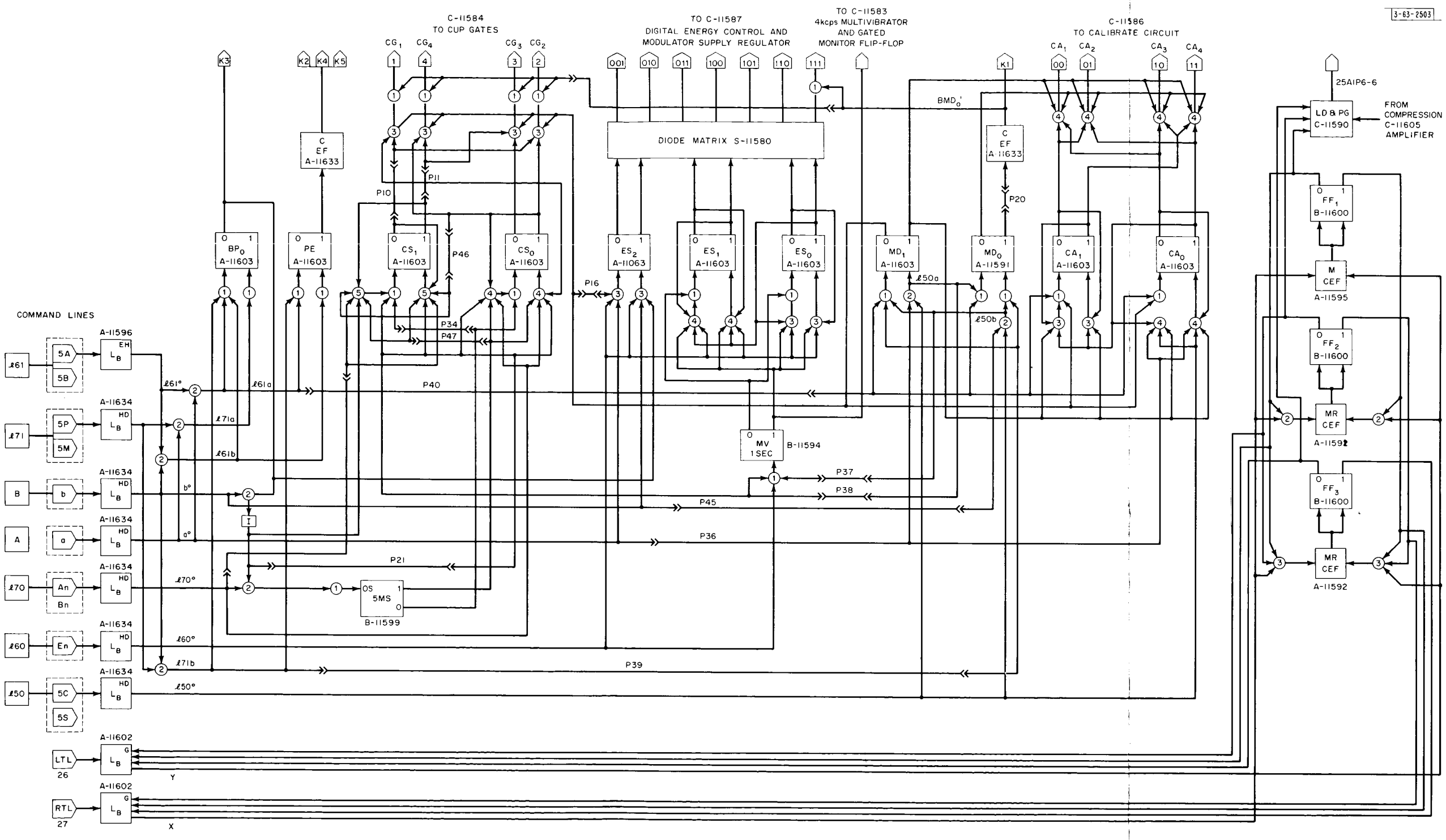


Fig. 26. Logic circuit, detailed block diagram.

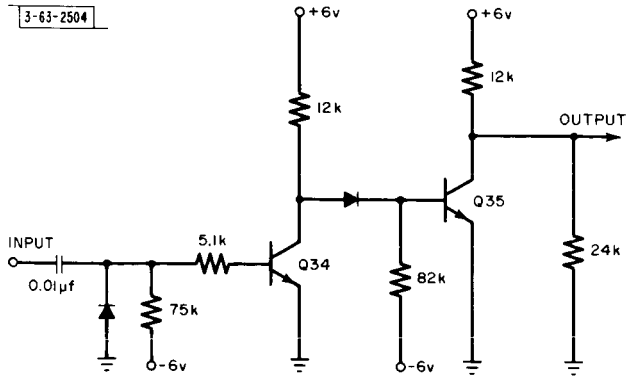


Fig. 27. Logic buffer.

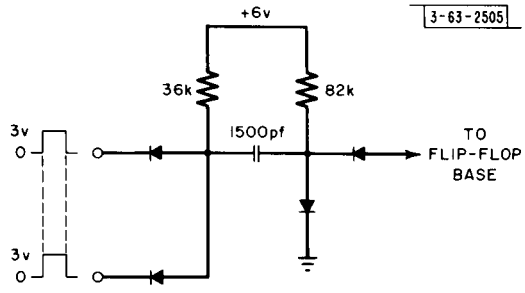


Fig. 28. "And" gate.

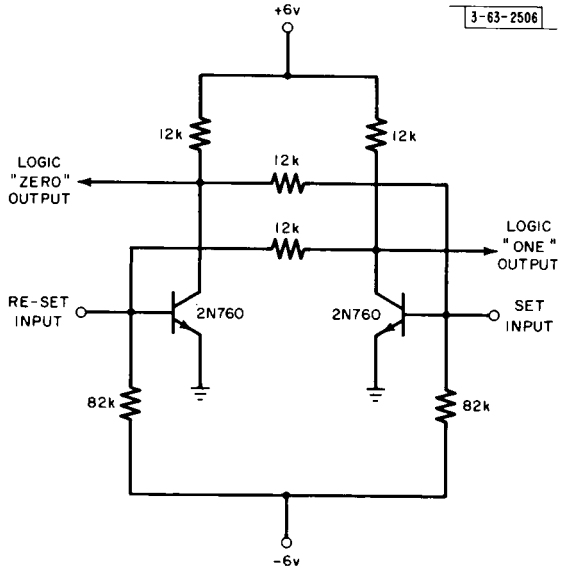


Fig. 29. Binary transistor flip-flop.

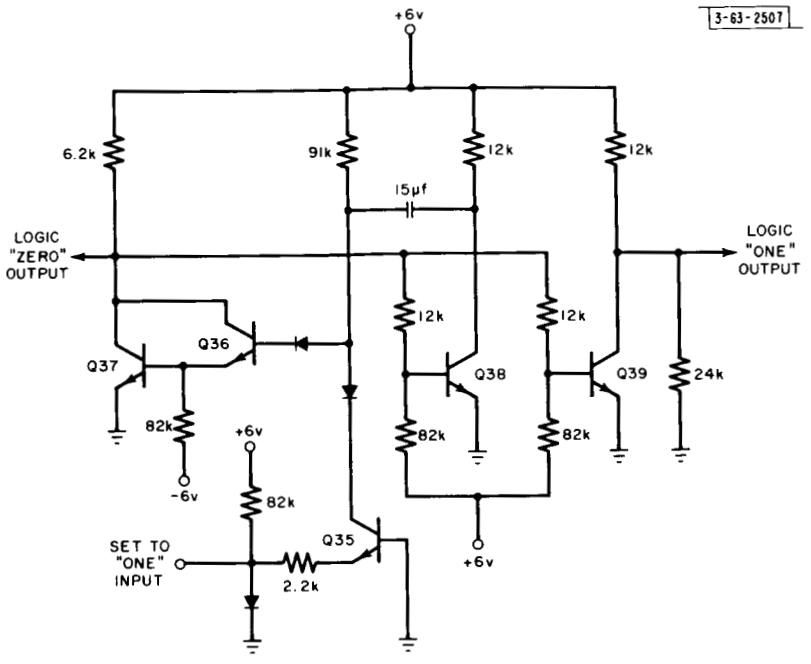


Fig. 30. Monostable multivibrator (1-μsec).

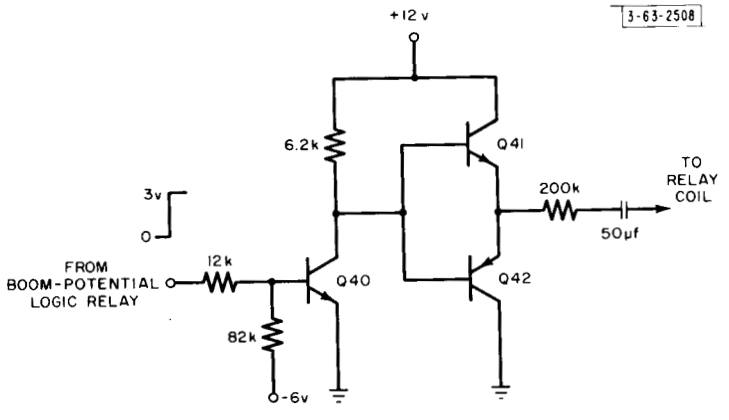


Fig. 31. Relay driver.

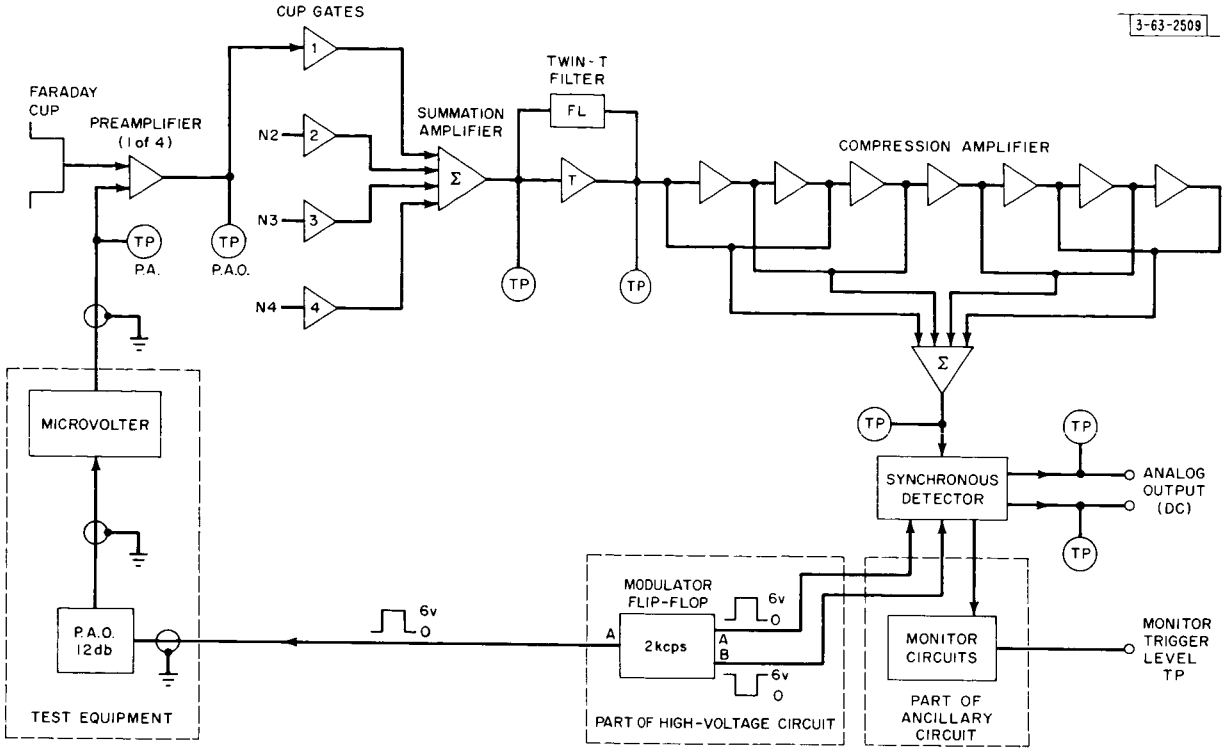


Fig. 32. Measurement link test setup.

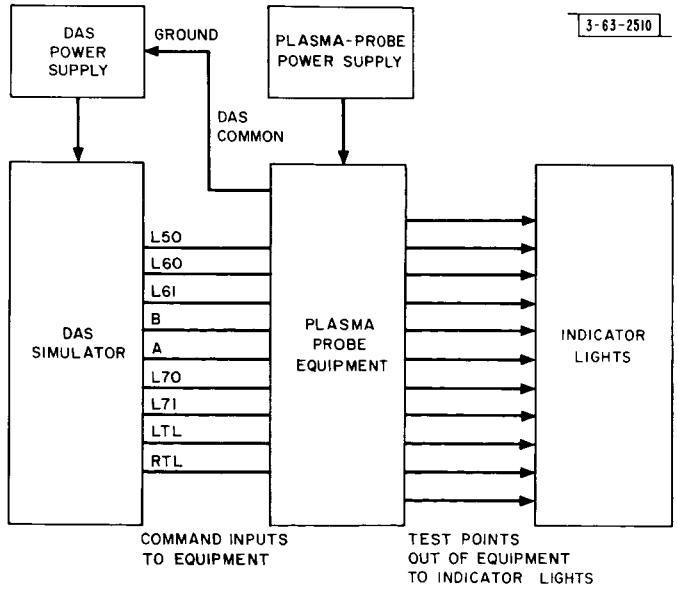


Fig. 33. Logic circuit test setup.

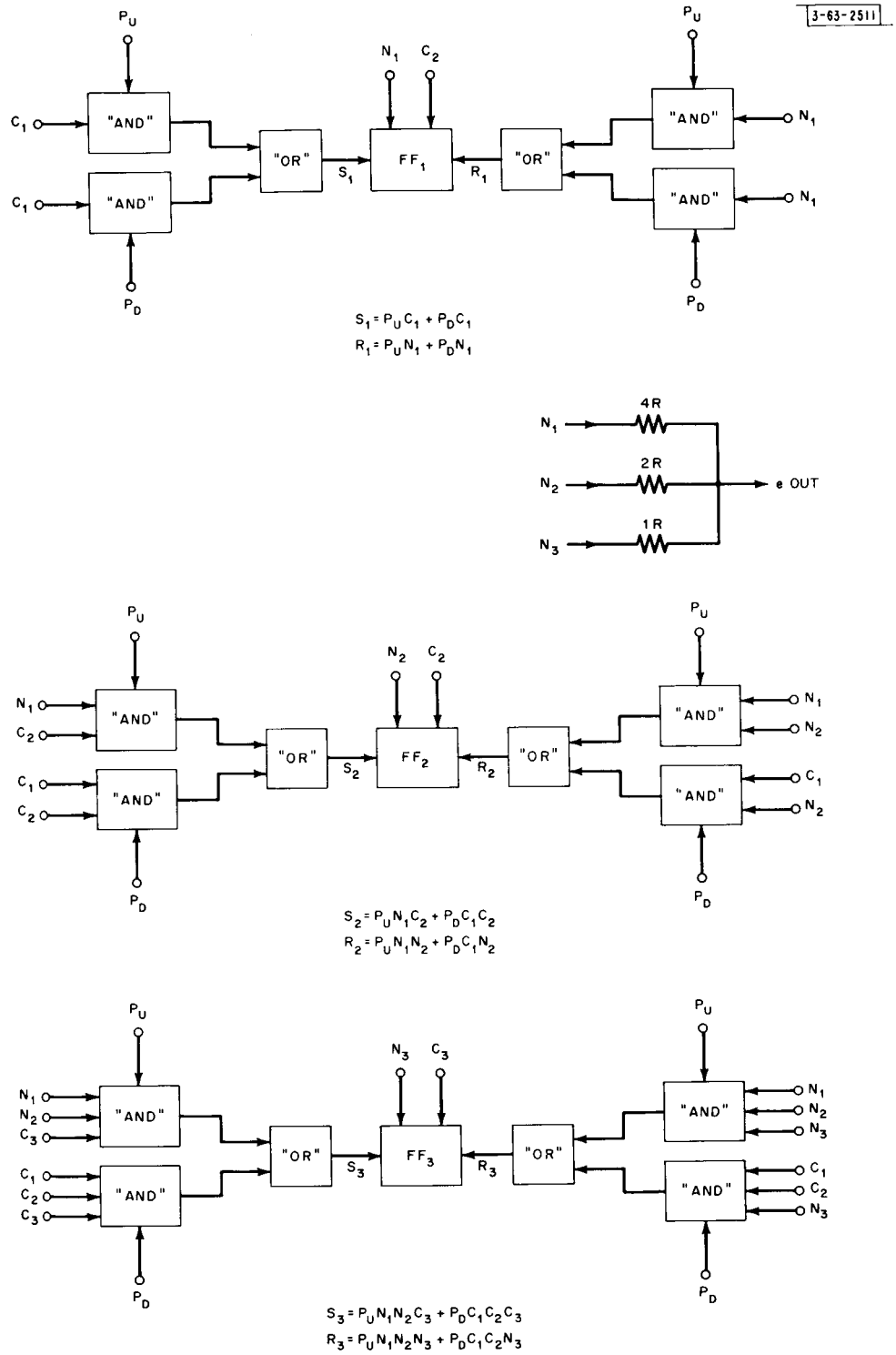


Fig. 34. Up-down binary counter.

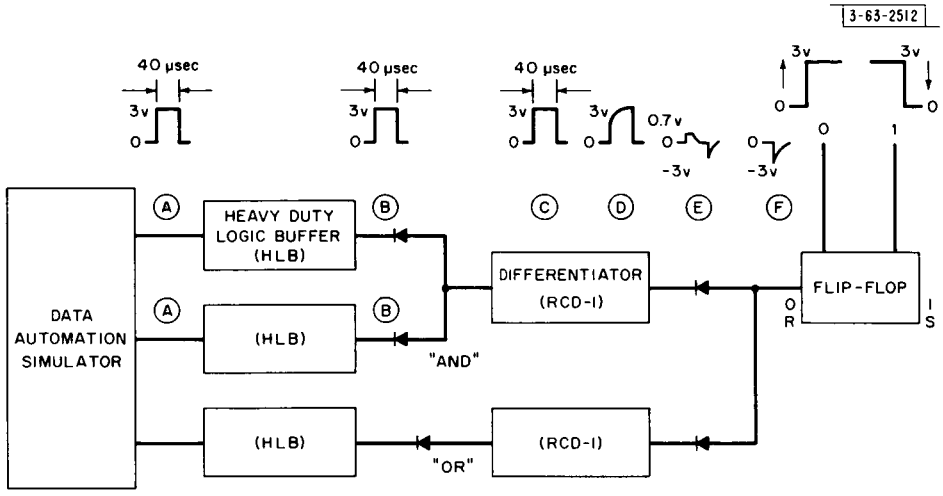


Fig. 35. Command circuit check points.